

GALLIUM ARSENIDE ON SILICON SUBSTRATE:  
GROWTH AND APPLICATION TO ELECTROOPTICAL DEVICES

By

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DEDICATED TO MY WIFE AND SON

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This dissertation describes a systematic study of heteroepitaxial growth of AlGaAs/GaAs films on silicon substrates and their application in achieving low loss optical waveguides and high efficiency phase modulators. A new atmospheric pressure metalorganic chemical vapor deposition (MOCVD) system was designed, constructed, and characterized for the growth of high quality AlGaAs/GaAs epitaxial layers on Si as well as GaAs substrates. Optimization of the growth parameters was carried out by material characterizations such as photoluminescence measurement, scanning electron micrograph, Hall mobility measurement, background carrier measurement, surface profile measurement, and surface morphology using a Normaski microscope. After optimization of growth parameters high quality GaAs epitaxial layers with a background carrier concentration of  $n = 1.4 \times 10^{14} \text{ cm}^{-3}$  and the electron mobility of  $\mu = 8100 \text{ cm}^2/\text{V}\cdot\text{sec}$  at  $300^\circ\text{K}$  were successfully grown on GaAs substrate.



The device quality GaAs film on Si substrates ( $n < 10^{15}$  cm<sup>-3</sup> and  $\mu > 5000$  cm<sup>2</sup>/V·sec at 300 °K) was obtained by using a sequential two step growth. It involves growing an optimum buffer layer thickness of 200 Å grown at 425 °C after annealing the substrate at 970 °C.

Finally, optical waveguides and phase modulators were designed, fabricated, and characterized, by using AlGaAs/GaAs-on-Si grown by molecular beam epitaxy (MBE) as well as MOCVD. Low loss GaAs waveguides on Si substrate with a average propagation loss of 1.2 dB/cm were demonstrated for the first time. This loss figure is comparable to that demonstrated with GaAs waveguides on GaAs substrates indicating that the dislocations due to the 4 % lattice mismatch are not a serious limitation. Two types of GaAs phase modulators on Si substrates were demonstrated: the p-n junction and Schottky barrier phase modulators with phase efficiencies of 3.5 °/V·mm and 4.7 °/V·mm, respectively. GaAs phase modulators on GaAs substrate were also studied for comparison purposes. According to our experimental results on the modulators using both GaAs and Si substrates as well as the theoretical analysis presented in this work, the thermally induced high stress in GaAs-on-Si does not seem to affect either the linear electro-optic effect or waveguide losses. These results indicate that the heteroepitaxially grown GaAs-on-Si is a viable alternative for electrooptical devices and for monolithic integration of low and high speed electronic and electrooptical devices.

## CHAPTER ONE

### INTRODUCTION

Since the invention of the transistor in 1947, the development of integrated electronic circuits has led to increased reliability with improved performance and reduced cost, size, weight, and power requirements of electronic devices and instruments. There has been a revolution in the electronics industry, in particular the computer industry, during the past decade due to advances made in integrated circuit technology.

The same advantages and enthusiasm have been responsible for a corresponding effort in integrated optical circuit technology, with the expectation of realizing similar benefits for communication, sensing, signal processing, and computing applications. Since light is used as a communication medium, integrated optics offer the advantages of huge available bandwidth and negligible sensitivity to interference by man-made electromagnetic fields of lower frequencies. Therefore, integrated optics will play a significant role in supplying the transition from an electronic technology to a future one that needs optical components for operating at optical frequencies. To provide all the function necessary in integrated optics such as waveguiding, modulation, detection, filtering, amplification,

and generation of light, photonic devices which can perform such operations on optical waves are essential to develop as optical counterparts of electronic devices in integrated electronics. During the past two decades, the field of integrated optics has grown rapidly; the result has been enormous progress in materials, fabrication process, component development, and device demonstration.

To date most of commercially available components in integrated optics are based on lithium niobate ( $\text{LiNbO}_3$ ) and extensive studies have been performed on  $\text{LiNbO}_3$  based integrated optics devices. However, significant resources are now going toward semiconductor-based integrated optics. The development of integrated optics in semiconductor materials is promising for higher levels of integration. An additional advantage is the integration compatibility of optical devices with electronics if silicon (Si) or gallium arsenide (GaAs) is the chosen substrate materials.

Gallium arsenide and its related compounds are particularly attractive because all the components necessary for signal transmission and processing such as waveguides, modulators, switches, amplifiers, lasers, and detectors can be accommodated on a common substrate. In analogy with the integrated circuit technology, these monolithically integrated devices are called optoelectronic integrated circuits (OEICs) [Mats83][Wada86]. The OEIC is believed to be the key device, not only for the next generation of optical communications [Forr85], but also for other innovations such

as optical computers. In high-speed information processing applications (for example, in board-to-board communication), it is expected that reasonably fast optical data transmission using OEIC will be needed even for short distances. Therefore, an eventual integration of all optoelectronic components on one chip, guided wave optical elements such as waveguides, modulators, couplers, and switches are essential.

One of the most basic components for integration is a low-loss optical waveguide which plays the role of interconnectors of various elements, as shown in Fig.1.1. Since light is guided in waveguide structures having dimensions close to that of a wavelength, small imperfections in the waveguide can be detrimental to the device performance. Research has started only recently in developing technology for fabrication of GaAs low loss optical waveguides [Lin85, Hiru85, Walk87, Kapo87, Seto90, Hibb90].

Moreover, since light waves are used as carriers for optical data transmission, ultra-high-speed photonic components are necessary to exploit the wide bandwidth available. On the transmitter end, a high speed modulator is needed to impress the electrical signal onto the light wave carrier. For this purpose, adequate GaAs waveguide modulators have to be developed and there has been vigorous research activity in this area as well [Alpi86, Wang87, Chen87].

The research efforts mentioned above have been strongly backed up by the rapid progress in the technologies which

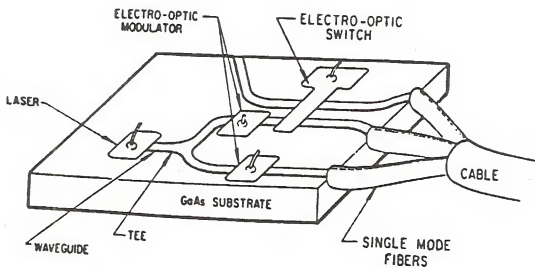


Figure 1.1 Waveguides used as the interconnectors in artist's sketch of a monolithic integrated GaAs transmitter. [Tami79]

have been developed for the growth of III-V semiconductor thin film epitaxial structures that are required for the realization of OEICs. In general, these growth techniques can be classified in three categories: (i) liquid-phase epitaxy (LPE), (ii) molecular beam epitaxy (MBE), and (iii) metalorganic chemical vapor deposition (MOCVD). None of the three methods meets all compound-semiconductor epitaxial needs, but a comparison of the three shown in Table 1.1 reveals the growing importance of the MOCVD growth technique.

LPE is a melt-growth technique. When a wafer is drawn across a melt of the desired material, an epitaxial layer solidifies as a result of supercooling [Dorr85]. Some advantages of LPE for the growth of III-V compounds are simplicity of equipment, higher deposition rates, high-quality film. Moreover, the technique is safe due to the elimination of hazards which may be caused if reactive gases were used since the gases and their reactive products are often toxic and explosive. LPE is also advantageous in growing certain structures which cannot be grown easily with either MBE or MOCVD because it is only possible to "fill in holes" with LPE: for example, buried heterostructure devices. Only recently, using a novel approach called CODE (compound orientation dependent epitaxy) technique in MOCVD [Scot88], which uses precursors selectively to deposit on particular surfaces but not on others, a buried heterostructure laser [Naru89] has been fabricated using single-step epitaxy.

Table 1.1 Comparison of epitaxial growth techniques

Technique	Characteristic			
	Solid composition	Purity	Advantage	Disadvantage
LPE	thermo-dynamics, (phase diagram)	III melt container	simple, high purity	higher impurity level, volume limited, poor morphology
MBE	kinetics, flux, sticking coefficient	vacuum sources, system (walls)	thin layer growth ( $<10\text{\AA}$ ), abruptness, low temperature growth, lattice mismatched growth	expensive, slow growth rate, problems with phosphorus oval defects
MOCVD	kinetics, arrival at surface	OM Sources, AsH <sub>3</sub> , C contamination, leaks	most versatile, large scale, very low impurity level, no oval defects, lattice mismatched growth	lack of <i>in situ</i> growth, toxic sources

However, there are some limitations in LPE technology, such as the non-uniformity of the layer thickness, roughness of the surface (poor morphology), and limitations on the wafer size. Owing to the high growth rate and melt-back effect, it is very difficult to grow multiquantum well (MQW) or superlattice structures with thickness less than 100 Å. Another critical limitation is the difficulty in growing epitaxial layers with carrier concentrations below  $10^{15} \text{ cm}^{-3}$  for application in most guided-wave optical components.

The advantage of MBE is that the growth process is controlled *in situ* by the use of on-line diagnostic equipments, such as pressure gauge, mass spectrometer, and electron diffraction facility etc., loaded within the MBE chamber[Dorr85]. MBE has attracted much interest as an excellent crystal growth technology, especially for AlGaAs/GaAs multilayer structures, because of its extremely precise control over layer thickness and doping profile, and the higher uniformity of the epitaxial layer over a large substrate area (2 ~ 3 inches in diameter). The disadvantages of MBE are that it employs a very expensive and complex technology, and that it has difficulties with p-type doping and in the growth of phosphorus-bearing alloys.

MOCVD technique, which is basically vapor phase epitaxy using metalorganic and hydride sources, is superior, or at least comparable to LPE and MBE in its abilities. The only disadvantages are safety caution due to the use of highly toxic sources and a lack of adequate *in-situ* monitoring of



the deposition reactions. However, it is significant to note that group-V hydrides, highly toxic gases such as arsine ( $\text{AsH}_3$ ) and phosphine ( $\text{PH}_3$ ), may soon be replaced by less toxic liquid metalorganic sources [Stri88]. For example, experiments with less toxic diethylarsine [Bhat87] have shown that pure GaAs films can be grown in an MOCVD reaction with trimethylgallium (TMGa). Such sources could improve safety in the MOCVD systems.

Together with the unique advantages of MOCVD such as mass production capability, wide-range controllability of the growth rate, excellent surface morphology, and repeatability of the growth of high-quality films, the most superior advantages for its applications to optical devices are the capability for growth of the undoped GaAs (background carrier concentration less than  $10^{14} \text{ cm}^{-3}$ ) [Inou85] and the ability to control Al-solid composition easily in AlGaAs. These abilities of MOCVD have enabled to fabricate low-loss GaAs optical waveguides (0.15 dB/cm) [Kapo87] and to control the refractive index very precisely. Also, the Al distribution coefficient in MOCVD grown AlGaAs layers is expected to be unity [Stri81].

As mentioned earlier, GaAs and Si are the most attractive substrates for OEIC's. As seen in Table 1.1, one of the most important technical breakthroughs has been the achievement of the heteroepitaxy with large lattice-mismatched material systems such as GaAs on Si substrate

[Wind84, Akiy84] and InP on Si [Lee87]. Only MOCVD and MBE are able to grow such mismatched heteroepitaxial layers since they are non-equilibrium growth techniques.

The heteroepitaxy involving growth of new mismatched, multimaterial systems mentioned above offers exciting applications. For example, AlGaAs/GaAs epitaxial layers on Si substrate offers a promising alternative for future optoelectronic devices, because of the possibility of combining the best material characteristics of GaAs with those of Si as shown in Table 1.2.

Silicon itself has many advantages over GaAs wafers as a substrate; large area, superior strength, high thermal conductivity, light weight, and low cost. Another major advantage is a well established processing technology for Si. On the other hand, GaAs is the most well known material for high speed electronic and optoelectronic devices, due to high mobility, direct energy-band gap, and electro-optic effect. Combination of these properties can replace the relatively expensive existing GaAs devices on GaAs substrates by the inexpensive heteroepitaxial GaAs devices on Si substrates with better characteristics such as higher heat dissipation capability. The most attractive point of this heteroepitaxy is the possibility of monolithic integration of Si (conventional inexpensive high density electronics) and GaAs (high speed electronic and opto-electronic devices) components within a single chip.

Table 1.2 Comparison of properties between Si and GaAs

	Si	GaAs
Crystal Structure	Diamond	Zinc-blende
Mechanical Strength	Strong	Weak
Cost	Cheap	Expensive
Specific Gravity	$2.33\text{g/cm}^3$	$5.32\text{g/cm}^3$
Wafer Size	8 ~ 10inch	3inch
Thermal Conductivity (300K)	$1.45\text{w/cm}\cdot\text{deg}$	$0.44\text{w/cm}\cdot\text{deg}$
Lattice Constant	$5.431\text{\AA}$	$5.653\text{\AA}$
Mobility	$1350\text{cm}^2/\text{V}\cdot\text{s}$	$8600\text{cm}^2/\text{V}\cdot\text{s}$
Transition	Indirect	Direct
$E_g$	1.11eV	1.43eV

This heteroepitaxy has already resulted in the development of a number of discrete optoelectronic and electronic devices, such as laser diodes [Kali87, Kim89], light-emitting diode [Flet84], photodetector [Pasi88], field-effect transistor [Aksu86], and bipolar transistors [Fisc86] etc., often exhibiting comparable performance characteristics similar to those of homoepitaxially grown devices (GaAs devices on GaAs substrate). Also as shown in Fig.1.2, some hybrid integration such as Si MOSFET-and-GaAs LEDs [Choi86] and Si MOSFETs-and-GaAs MODFETs [Fisc85], have already been demonstrated.

However, in spite of the importance of guided-wave elements as mentioned earlier, research on these GaAs guided-wave components on Si has not been reported yet. Therefore, it is necessary to study various optical components using GaAs-on-Si like waveguides and modulators for an ultimate monolithic integration on Si substrate. Even though the viability of lasers using GaAs-on-Si (performances and reliability) is yet to be proven, nevertheless, considering the possibility of high speed signal processing with an external light source, we believe that heteroepitaxially grown optical devices are likely to play an important role in the OEICs of tomorrow.

In this work, we describe the studies of GaAs heteroepitaxy on Si by MOCVD, and results on the development of low-loss GaAs/AlGaAs optical waveguides [Kim88, Kim89] and

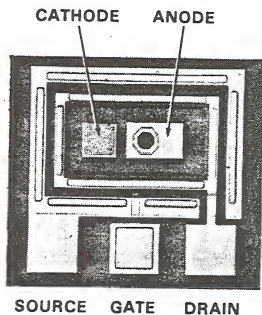
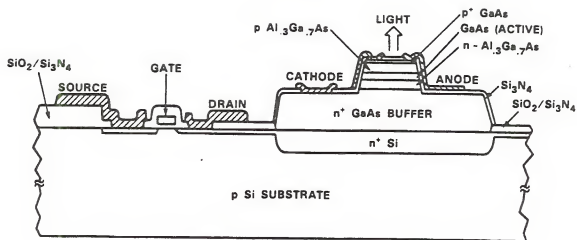


Figure 1.2 An Example of hybrid integration by use of GaAs-on-Si [Choi86]. Schematic cross-sectional diagram of a monolithically integrated Si MOSFET and GaAs/AlGaAs LED (top) and optical micrograph of a GaAs LED and surrounding Si MOSFET.

GaAs/AlGaAs phase modulators [Kim89, Kim90] in this material system.

This dissertation consists of a total of seven chapters. Following this chapter on introduction, the basics of the MOCVD technology related to the present study are described in chapter two. In chapter three, the design concepts, actual construction work, and description of the AlGaAs/GaAs ternary MOCVD system at the University of Florida will be explained in detail. Chapter four covers the characterizations of epitaxial layers carried out for defining the optimum growth parameters in our MOCVD system. In chapter five, after describing the properties of GaAs-on-Si, we explain the growth of GaAs-on-Si. In chapter six, as an application to optical devices, studies on AlGaAs/GaAs waveguides and phase modulators on Si substrates will be described. Finally, chapter seven contains a summary of the present study. Suggestions for future work are also included in this chapter.

## CHAPTER TWO

### BASICS OF METALORGANIC CHEMICAL VAPOR DEPOSITION

This chapter is intended to be a comprehensive summary of the metalorganic chemical vapor deposition(MOCVD) of III-V semiconductors which forms the background of this work. After historical and brief introduction including the fundamental aspects of MOCVD growth in the first section, some fundamental properties of GaAs and AlGaAs grown by MOCVD will be explained in the second and third section.

#### 2.1 Introduction

MOCVD, a process for the deposition of compound semiconductor thin films, was introduced in 1968 by Manasevit [Mana68]. The term "MOCVD" was originated in order to emphasize that the process transported metals using organic compounds, hence "metalorganic(MO)" rather than the more rigorously correct "organometallics". The first experiments utilized such insulating substrates such as glass and sapphire ( $\text{Al}_2\text{O}_3$ ) and produced GaAs by using TMGa(or TEGa) and  $\text{AsH}_3$  as the sources of Ga and As respectively [Mana68, Mana68]. Because these films were not true epitaxial films (oriented to the substrate lattice), the more general term deposition rather than epitaxy was used. Soon after

Manasevit's first demonstration, true epitaxial single-crystal GaAs on GaAs substrate was produced by Rai-Choudhury [Rai-69].

Today, MOCVD is an important epitaxial technology for several basic reasons. For example, all constituents are in the vapor phase which allows for accurate electronic control of important system parameters such as gas flow rates and, hence, partial pressures. The pyrolysis reaction is relatively insensitive to growth temperature, allowing for efficient and reproducible deposition of thin layers and abrupt interfaces between deposited layers. Commercial adaption of research reactors is a reality now since a scaling to production volumes is simpler to achieve than with the other epitaxial growth methods.

By mixing metal alkyls and hydrides of different elements, binary, ternary and quaternary III-V, II-VI, and IV-VI compounds can be formed in a manner analogous to GaAs. However, most of the work to date have been concentrated on the III-V compounds, in particular, on GaAs and  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ . Table 2.1 lists the various III-V compound semiconductors that have been grown epitaxially by MOCVD. Fig.2.1 shows that vapor pressures of common metal alkyls, the most important property used in the MOCVD growth of III-V compound semiconductors. All of metal alkyls and hydrides used as reactants are flammable, pyrophoric (severely reacting with water and air), or toxic. Therefore appropriate precautions must be taken in their handling.



Table 2.1 III-V semiconductors grown by MOCVD

Material	Reactants
AlAs	TMA1 - AsH <sub>3</sub>
AlN	TMA1 - NH <sub>3</sub>
GaAs	TMGa - AsH <sub>3</sub> TEGa - AsH <sub>3</sub> DEGaCl - AsH <sub>3</sub>
GaN	TMGa - NH <sub>3</sub>
GaP	TMGa - PH <sub>3</sub> TEGa - PH <sub>3</sub>
GaSb	TEGa - TMSb
InAs	TEIn - PH <sub>3</sub>
InP	TEIn - PH <sub>3</sub> TMIn - PH <sub>3</sub>
InSb	TMIn - SbH <sub>3</sub>
Al <sub>x</sub> Ga <sub>1-x</sub> As	TMGa - TMA1 - AsH <sub>3</sub> TEGa - TMA1 - AsH <sub>3</sub>
GaAs <sub>1-x</sub> P <sub>x</sub>	TMGa - AsH <sub>3</sub> - PH <sub>3</sub>
GaAs <sub>1-x</sub> Sb <sub>x</sub>	TMGa - AsH <sub>3</sub> - SbH <sub>3</sub> TMGa - TMSb - AsH <sub>3</sub>
Ga <sub>1-x</sub> In <sub>x</sub> As	TMGa - TEIn - AsH <sub>3</sub>
InAs <sub>1-x</sub> P <sub>x</sub>	TEIn - AsH <sub>3</sub> - PH <sub>3</sub>
Ga <sub>1-x</sub> In <sub>x</sub> As <sub>1-y</sub> Py	TEIn - TMGa - PH <sub>3</sub> - AsH <sub>3</sub>

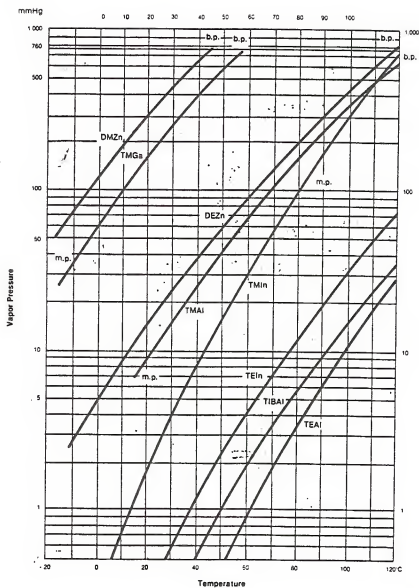


Figure 2.1 Vapor pressure curves for various metal alkyls [Mort86].

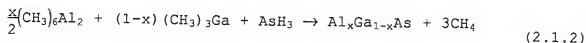
Growth of III-V epitaxial semiconductors by MOCVD takes place by introducing metered amount of the group III alkyls and group V hydrides in a carrier gas into a quartz reaction tube which contains a substrate placed on a heated susceptor surface. The hot susceptor has a catalytic effect on the decomposition of the gaseous products and the growth rate is proportional to the flow rate of the group III species, but it is independent of the partial pressure of group V species. The gas molecules diffuse across the boundary layer of the laminar flow zone [Ban78] to the substrate surface where the metal alkyls and hydrides decompose to produce the group III and group V elemental species. The elemental species move on the hot surface until they find an available lattice site where growth then occurs. However, the exact chemical decomposition pathways in MOCVD are not yet clearly understood. The nature of the reactions is known to be partly determined by the velocity and temperature profiles near the susceptor and subsequent concentration and thermal gradient that are established. Of course, the reaction pathways are also strongly influenced by the choice of precursor chemicals.

Although the reaction chemistry is complex and contains contributions from homogeneous and heterogeneous pyrolysis, the basic overall reaction chemistry using group-III metal alkyls and group-V hydrides can be summarized in general form as follows:



,where R : an organic radical  
 M : group-III metal element  
 X : group-V element  
 n : integer

For example, the overall reaction of TMGa, TMAI, and AsH<sub>3</sub> to yield Al<sub>x</sub>Ga<sub>1-x</sub>As is:



Depending primarily upon precursor selection, reactor pressure, system design details, methods of mixing the chemicals in the gas stream, and the carrier gas composition, distinguished variations in the technique can be utilized to improve the film characteristics.

## 2.2 Growth of GaAs

One of the inherent features of the GaAs growth can be summarized by stating that the growth rate is directly proportional to the group III alkyl input flux at atmospheric pressure [Mori81, Aebi81, Reep83], largely independent of the substrate orientation [Reep83, Saxe81], and nearly constant over the growth temperature range (600 ~ 850 °C) under AsH<sub>3</sub>-rich conditions. According to the study of the growth rates in the wide range of growth temperature (400 ~ 1000

°C) [Reep83], there are three different growth regimes, each with a characteristic growth mechanism.

At temperature below 600 °C, the reaction is mass transport limited. There are several different points of view regarding the rate-limiting factor. One report shows that AsH<sub>3</sub> adsorption, enhanced by TMGa adsorption, appears to be the rate-limiting step below 600 °C [Reep83]. Others suggest that the cracking rate of TMGa [Tsan84] or AsH<sub>3</sub> pyrolysis [Dapk81, Esco82] becomes limiting factor. There is no resolution yet between these conflicting viewpoints.

At temperatures exceeding 850 °C, the growth rate is controlled by the sticking coefficients of the group V species and by the total reactant input rate. More gas phase nucleation occurs which tends to favor polycrystalline, rather than single crystal growth. The rate-limiting step in this region is believed to be the decomposition of the surface by desorption of Ga [Reep83] or As [Stri78] or the premature decomposition of the precursors homogeneously in the gas leading to parasitic decomposition on the reactor walls [Leys81].

In the useful intermediate temperature range between 600 °C and 850 °C, growth is mass-transport limited by the diffusion of TMGa through the boundary layer over the susceptor, provided there is sufficient AsH<sub>3</sub> overpressure. The growth rate tends to increase slightly toward the 850 °C limit. The lower limit of the middle range can be extended to 500 °C by precracking the AsH<sub>3</sub> to As<sub>2</sub> and As<sub>4</sub> before the gas

stream reaches the susceptor [Krae83]. Also, it is known that the growth rate is independent of the  $\text{AsH}_3$  partial pressure under conditions of excess  $\text{AsH}_3$  ( $\text{AsH}_3/\text{TMGa} > 1$ ) [Bass75, Duch79, Reep83, Krae83]. In the following, we describe the properties of GaAs grown by MOCVD at intermediate temperatures (600 ~ 850 °C) only.

### 2.2.1 Purity of GaAs

A typical plot of the background doping as a function of inlet V/III ratio is shown in Fig.2.2. The free carrier background of unintentionally doped GaAs changes from p to n type as the  $\text{AsH}_3/\text{TMGa}$  ratio is increased [Ito73, Wata83]. However, there is a wide variation in the value of the ratio where the background changes from p to n type under a variety of conditions using different reactor and sources [Taka83, Taka84]. Major factors that affect the purity of MOCVD grown GaAs are source purity, reactor cleanliness, and growth conditions. There have been many attempts to investigate dominant impurities. It is believed that they are water, carbon, silicon, and zinc. Carbon as the dominant residual acceptor coming from the  $\text{CH}_3$  associated with the TMGa [Samu81, Koba82, Leys81], although other organic contaminants [Davi84] in the TMGa may also contribute to carbon contamination. It is reported [Koba82] that an increase in As vacancies at reduced  $\text{AsH}_3/\text{TMGa}$  ratio causes enhanced C incorporation on As(acceptor) sites. Also, Zn was found to be

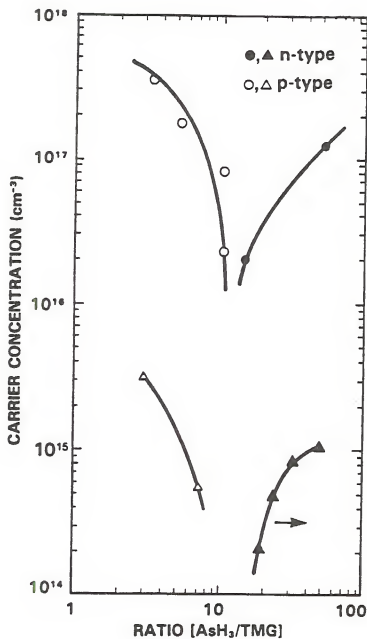


Figure 2.2 Typical plots of the background carrier concentration of GaAs grown by MOCVD as a function of inlet AsH<sub>3</sub>/TMGa ratio [Ito73, Wata83].

the dominant background acceptor in more contaminated GaAs, otherwise C predominates. As the dominant n-type background impurity, Si with Ge, Sn, S, and Te were identified.  $H_2O$  contained in  $AsH_3$  act as n-type background dopant. However, it is confirmed that TMGa rather than  $AsH_3$  or reactor components contribute to the dominant background impurities [Hess82]. Other impurities, such as oxygen, appear to have little or no effect on GaAs growth by MOCVD. The purest GaAs grown by MOCVD so far reported has a background doping of  $n=6.5 \times 10^{13} \text{ cm}^{-3}$  and a mobility  $\mu=210,000 \text{ cm}^2/\text{V}\cdot\text{sec}$  at 77K [Shas88].

#### 2.2.2 Doping Concentration

The behavior of dopant incorporation in MOCVD process can be classified into two distinct categories[Raze83]: (a) all the cracked species incorporate into the growing layer regardless of the growth rate (mass transport limited); and (b) the small fraction of incorporated dopant is controlled by a balance between evaporation back into the gas and attachment to a lattice site (surface kinetic limited). Elements which have a relatively high vapor pressure at the growth temperature such as Zn, Se, Cd, and S behave according to the second case, whereas those with low vapor pressure such as Si, Ge, and Sn behave according to the first case.

The most often used p-type dopant is Zn. The MO sources of Zn are diethylzinc (DEZn) and dimethylzinc (DMZn). It is known that the Zn-doping levels by these sources depend on



the growth temperature, III/V ratio, growth rate, and reactor design [Aebi81, Bass77]. The highest achievable level of hole concentration in GaAs by Zn dopants is  $1 \times 10^{19} \text{ cm}^{-3}$  [Aebi81]. As p-type dopants, Mg and Be have also been used [Lewi83, Pars83]. Bis-cyclopentadienyl-magnesium ( $\text{Cp}_2\text{Mg}$ ) and dimethyl- or diethyl-berilium (DMBe or DEBe) are the sources of Mg and Be dopants, respectively. These sources have higher doping efficiency than Zn due to the lower vapor pressure at the growth temperature. The highest p-type doping levels in GaAs by MOCVD have been achieved by the use of DMBe ( $p = 2.3 \times 10^{20} \text{ cm}^{-3}$ ) [Mell81] and DEBe ( $p = 1.6 \times 10^{20} \text{ cm}^{-3}$ ) [Pars83]. The highest doping level for Mg is  $2 \times 10^{19} \text{ cm}^{-3}$  [Lewi83]. However, they are not widely used since Mg reactant is easy to adsorb onto the reactor components and Be compounds are notoriously toxic.

As the n-type dopants in MOCVD,  $\text{Si}(\text{SiH}_4)$  and  $\text{Se}(\text{H}_2\text{Se})$  are used most often. The electron concentration using either of the two dopants is dependent on growth temperature, growth rate and reactor. The free carrier concentration for Si doping is independent of  $\text{AsH}_3$  concentration for low pressure MOCVD, while that for Se doping varies as a function of  $\text{AsH}_3$  concentration [Duch79, Keil82]. The Si doping efficiency (less than  $10^{18} \text{ cm}^{-3}$ ) is relatively lower than Se ( $n = 1.5 \times 10^{19} \text{ cm}^{-3}$ ). Thus, very high input flux of  $\text{SiH}_4$  is needed for high doping. In that case, it is known that the mobilities drop rapidly due to the compensation of the material [Ludo85]. In the case of  $\text{H}_2\text{Se}$ , since  $\text{H}_2\text{Se}$  is a polar molecule, it tends to adsorb and desorb off the reactor walls. This leads to a memory effect

[Lewi84] when the dopants are changed abruptly. This problem is not seen with  $\text{SiH}_4$ .

### 2.3. Growth of $\text{Al}_x\text{Ga}_{1-x}\text{As}$

There is great similarity between the growth of GaAs and  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ , together with simple substitution of TMAI for TMGa in the gas and Al for Ga in the solid. Over a wide range of substrate temperatures ( $600 \sim 850^\circ\text{C}$ ) and  $\text{AsH}_3$  overpressure, there is a close correspondence between the vapor and solid compositions of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ . Fig.2.3 shows the Al mole fraction as a function of the input concentration ratio  $[\text{TMAI}]/[\text{TMAI}+\text{TMGa}]$  according to the data taken from several sources [Aebi81, Taka83, Mori81, Cole81]. A notable tendency for the Al composition is the unit proportionality to the gas-phase composition. Another property is that the growth rate of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  increases with  $x$ , as shown in Fig.2.4. At a given Al mole fraction  $x$ , the growth rate is proportional to the total alkyl concentration in the reactor, and largely independent of substrate temperatures ( $600 \sim 850^\circ\text{C}$ ).

The quality of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  deposited by MOCVD is extremely sensitive to the unintentional incorporation of residually originated impurities in the input gas stream. This is basically caused by the very strong Al-O bond which causes  $\text{O}_2$  and  $\text{H}_2\text{O}$  in the vapor phase to adsorb onto the growing interface and be incorporated into the solid. Most of  $\text{O}_2$  and  $\text{H}_2\text{O}$  comes from the  $\text{AsH}_3$ . Various methods have been used for

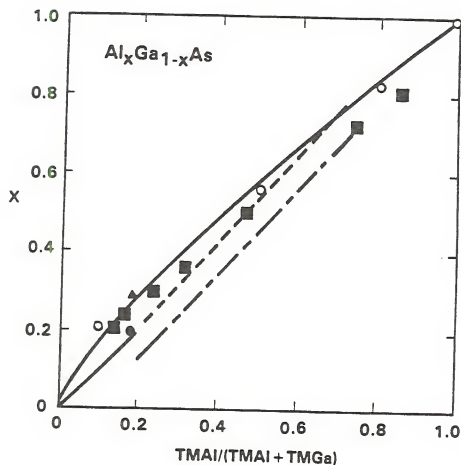


Figure 2.3 Solid composition  $x$  of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  as a function of the input concentration ratio  $[\text{TMAI}]/[\text{TMAI} + \text{TMGa}]$ . Data taken from [Aebi81] (○), [Taka83] (▲ = low  $\text{H}_2$  flow, ● = high  $\text{H}_2$  flow), [Mori81] (for horizontal (·····) and vertical (----) reactor, and [Cole81] (■) for vertical reactor.

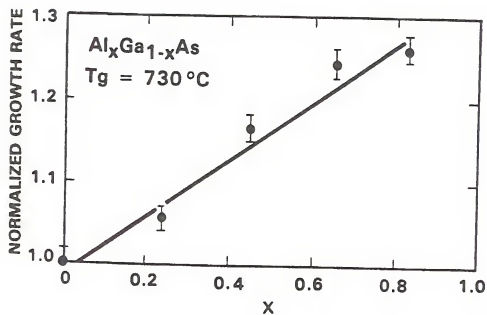


Figure 2.4 Normalized growth rate of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  as a function of composition  $x$ .

removal of water and oxygen from arsine *in situ*. These include graphite baffles [Stri81, Tsai84], molecular sieves [Thru79, Hoof81], an Al/Ga/In eutectic alloy bubbler in AsH<sub>3</sub> [Shea83, Kim86], dry ice cold trap [Fraa85, Part85], gettering buffer layers of Al<sub>x</sub>Ga<sub>1-x</sub>As [Hers82], and substitution of 100% arsine for the usual dilutions in hydrogen carrier gas [Naka84]. High temperature growth has also been found to be effective in improving the quality of the Al<sub>x</sub>Ga<sub>1-x</sub>As epitaxial layers [Tsai84].

Dopants of Al<sub>x</sub>Ga<sub>1-x</sub>As behave similar to GaAs. As a characteristic behavior for Zn (DEZn) in Al<sub>x</sub>Ga<sub>1-x</sub>As the hole concentration dependent on  $x$  is shown in Fig.2.5.

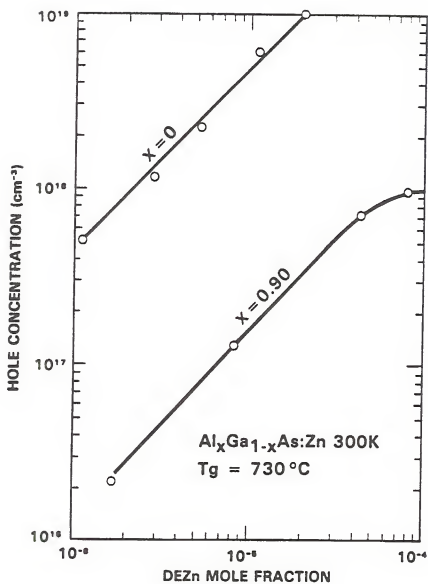


Figure 2.5 Doping characteristic of Zn in  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  [Aebi81].

## CHAPTER THREE

### MOCVD SYSTEM

This chapter describes the design and construction of the MOCVD system used in the present study. The first section deals with the design concepts. The actual construction including the selection of critical parts and description of MOCVD system will be explained in detail in the final section.

#### 3.1 Design Concepts

##### 3.1.1 Introduction

The atmospheric pressure AlGaAs/GaAs ternary MOCVD system at the University of Florida was designed to grow various AlGaAs/GaAs optical and optoelectronic device structures as well as high quality epitaxial layers. The initially proposed device structures were double-hetero(DH) structure lasers with various operating wavelengths, single and multi-quantum-well structure lasers, graded index separate confinement hetero-structure(GRINSCH) devices, and various optical waveguide structures. Together with the general requirements of the MOCVD system for the growth of

high quality AlGaAs/GaAs epitaxial layers, specific requirements based on such device structures were considered for the actual design. Some general requirements are: precise thickness control, abrupt interfaces, uniformity, low density of defects, and control of carrier concentration.

After considering specific requirements for the growth of various desired structures, possible configurations of the Al and Ga lines and the simulation of flow rate will be discussed. Design considerations to fulfil the general requirements will be explained in the following subsections.

### 3.1.2 Specific device considerations

#### DH lasers:

For the growth of DH lasers with various operating wavelengths, an abrupt change of Al mole fraction should be carried out at the interface during the sequential growth of the cladding layers and active layer. To achieve this kind of operation without interrupting the growth sequence, at least two independently controlled Al source lines are desirable. Also for the growth of the  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  active layer with small Al mole fraction such as  $x=0.05$ , an accurate control of the Al flow should be guaranteed at low flow rates.

#### MQW laser:

An abrupt change of the growth rate is required for the transition from the thick cladding layer to the MQW active



layers. Therefore at least two independently controlled Ga lines are needed as well as two Al lines for the sequential growth. For the very low growth rate of MQW layers, each of the two lines should be capable of handling very low flow rates.

#### GRINSCH:

Gradual changes of Al and Ga flow rates are required with a wide range of controllability of the flow rates.

#### Optical waveguides:

All the restrictions of Al and Ga control mentioned above should be satisfied for growing the various structures for optical waveguides. Another fundamental requirement is the capability to grow materials with carrier concentrations less than  $10^{15} \text{ cm}^{-3}$ . For the fulfillment of this condition, impurity levels and memory effect of the MOCVD system should be carefully handled during the design and construction phases. These considerations requiring special care will be discussed in the following sections and in the next chapter.

#### 3.1.3 Simulation of flow rates

Based on the discussion in subsection 3.1.2., two Ga lines and two Al lines were chosen for the alkyl sources. As alkyl sources, TMGa and TMAI were selected. Since the growth is carried out under As-rich conditions, one As line is

adequate for the system. Examples of proposed device structures shown in Table.3.1 were used for the simulation of the flow rates.

The growth rate and uniformity of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  as a function of composition can be modeled quite successfully by simply using the gas law and considering the nature of the steady-state gas-flow characteristics in the reactor. The MOCVD process is almost always carried out under conditions of excess arsine, so that the limiting mass-transfer components are the metal alkyls, namely, TMGa and TMAI. Assuming that the metal-alkyl pyrolysis efficiencies are unity, the growth rate  $g$  is given by [Dapk82]

$$g = k(T) \{ (\text{MF})_{\text{Ga}} + 2(\text{MF})_{\text{Al}} \} \quad (3.1.1)$$

,where  $(\text{MF})_{\text{Ga}}$  and  $(\text{MF})_{\text{Al}}$  are mole fractions of TMGa and TMAI, respectively. The composition  $x$  of the grown MOCVD epitaxial  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  layer is simply determined from the mole fraction ratio of TMGa and TMAI and is given by

$$x = \frac{2(\text{MF})_{\text{Al}}}{(\text{MF})_{\text{Ga}} + 2(\text{MF})_{\text{Al}}} \quad (3.1.2)$$

The factor of 2 used to multiply the TMAI vapor pressure results from the fact that TMAI is a dimer. In Eq.(3.1.1), the term  $k(T)$ , where  $T$  is the growth temperature, represents mainly a geometric correction factor which includes an

Table 3.1 Proposed device structures used for the simulation of the flow rates

(a) DH laser		Substrate/GaAs (2 $\mu$ m) /Al <sub>0.3</sub> Ga <sub>0.7</sub> As (2 $\mu$ m) /Al <sub>0.05</sub> Ga <sub>0.95</sub> As (0.05 $\mu$ m) /Al <sub>0.3</sub> Ga <sub>0.7</sub> As (2 $\mu$ m) /GaAs (0.5 $\mu$ m)
(b) Superlattice laser		Substrate/GaAs (2 $\mu$ m) /Al <sub>0.6</sub> Ga <sub>0.4</sub> As (2 $\mu$ m) / [GaAs/Al <sub>0.2</sub> Ga <sub>0.8</sub> As] <sup>n</sup> (100Å/100Å) <sup>n</sup> /Al <sub>0.6</sub> Ga <sub>0.4</sub> As (2 $\mu$ m)/GaAs (0.5 $\mu$ m)
(c) GRINSCH		Substrate/GaAs (2 $\mu$ m) /Al <sub>0.6</sub> Ga <sub>0.4</sub> As (2 $\mu$ m) / $\Delta$ Al <sub>0.6</sub> $\rightarrow$ 0.2Ga <sub>0.4</sub> $\rightarrow$ 0.8As (0.2 $\mu$ m) /GaAs (100Å) / $\Delta$ Al <sub>0.2</sub> $\rightarrow$ 0.6Ga <sub>0.8</sub> $\rightarrow$ 0.4As (0.2 $\mu$ m) /GaAs (0.5 $\mu$ m)
(d) Waveguide	d-1	Substrate/Al <sub>0.05</sub> Ga <sub>0.95</sub> As (2 $\mu$ m) /GaAs (2~6 $\mu$ m) /Al <sub>0.05</sub> Ga <sub>0.95</sub> As (2~5 $\mu$ m)
	d-2	Substrate/Al <sub>0.05</sub> Ga <sub>0.95</sub> As (2 $\mu$ m) /GaAs (5 $\mu$ m) /Al <sub>0.05</sub> Ga <sub>0.95</sub> As (2 $\mu$ m) / [GaAs/Al <sub>0.3</sub> Ga <sub>0.7</sub> As] <sup>n</sup> (100Å/100Å) <sup>n</sup> /Al <sub>0.05</sub> Ga <sub>0.95</sub> As (2 $\mu$ m) /GaAs (5 $\mu$ m)

effective area term that accounts for parasitic deposition elsewhere in the reactor. This term is essentially constant in the intermediate temperature range (600 ~ 850 °C). Total mole fraction of group III is given by

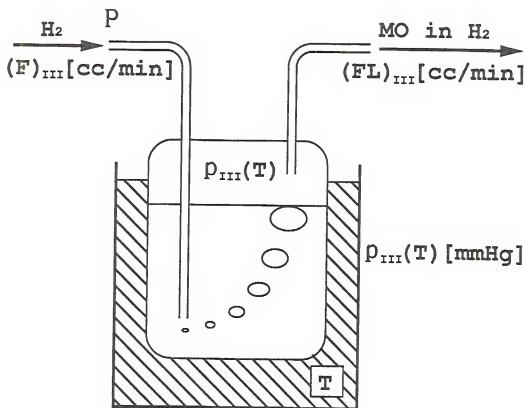
$$\begin{aligned} (MF)_{III} &= (MF)_{Ga} + 2(MF)_{Al} \\ &= (FL)_{III} / (F)_T \end{aligned} \quad (3.1.3)$$

, where  $(FL)_{III} = (FL)_{Ga} + 2(FL)_{Al}$   
 $(FL)_{Ga}$  and  $(FL)_{Al}$  are the flow rates of TMGa and TMAI out of each bubbler, respectively.  $(F)_T$  is the total flow rate of hydrogen. Thus the flow rates of hydrogen through the metal alkyl bubblers can be determined by the following relation as shown in Fig.3.1.

$$(F)_{III} = \frac{P \times (FL)_{III}}{p_{III}} \quad (3.1.4)$$

, where  $P$  is the pressure of bubbler inlet and  $p_{III}$  is the vapor pressure of the metal alkyls. In summary,  $P$ ,  $p_{III}$ ,  $(F)_T$ ,  $x$ ,  $k$ , and  $g$  are the parameters for the simulations of  $(F)_{Ga}$  and  $(F)_{Al}$ .

In this simulation, 10 slm total flow of H<sub>2</sub> and empirical value of  $k = 650$  are used based on the reactor data provided by Japan Oxygen Inc.. Also vapor pressures at 0 °C and 20 °C are used for TMGa and TMAI, respectively.  $P$  was



$$(FL)_{III} = \frac{p_{III}}{P} \times (F)_{III} \quad [\text{cc/min}]$$

Figure 3.1 Flow of H<sub>2</sub> through the metal alkyl bubbler

chosen on the basis of special MO lines schematic explained in the next subsection. Growth rates are chosen optimally for each proposed device structures. The results of the simulation are shown in Table 3.2. According to the results, 20 sccm and 100 sccm mass flow controllers(MFC) are necessary for each metal organic line. MFC with maximum flow rate of 100 sccm for AsH<sub>3</sub> line has been determined for the system, by use of the following relation.

$$(F)_V = (MF)_{III} \times \left( \frac{V}{III} \right) \quad (3.1.5)$$

,where (V/III) indicates the mole fraction ratio of group III and group V elements.

#### 3.1.4 Consideration for thickness and abruptness

Small variations of thickness and abruptness of the epitaxial layers may not be critical for a device with thick epitaxial layers. However, for devices with thin layers like MQW structure (with thickness less than 100 Å), even small variations could affect the device performance seriously. Since growth rate is essentially proportional to the supply of the reactants that provide the group III elements, decreasing the supply of these reactants will in principle make the growth rate arbitrarily small. By changing the gas composition, very thin layers (<100Å) with abrupt

Table 3.2 (Part 1) The results of the simulation (*continued*)

Growth conditions (flow rate)													Total flow=10SLM
structure	material	thickness ( $\mu\text{m}$ )	time (min)	Al1		Al2		Ga1		Ga2		III/H2	growth rate ( $\mu\text{/min}$ )
				sccm	MF	sccm	MF	sccm	MF	sccm	MF		
a	GaAs	2	10	-	-	-	-	66	3.1E-4	-	-	3.1E-4	0.2
	Al <sub>0.3</sub> Ga <sub>0.7</sub> As	2	8	32	6.7E-5	-	-	66	3.1E-4	-	-	3.77E-4	0.25
	Al <sub>0.05</sub> Ga <sub>0.95</sub> As	0.1	0.5	-	-	3.9	8.1E-6	66	3.1E-4	-	-	3.18E-4	0.21
	Al <sub>0.3</sub> Ga <sub>0.7</sub> As	2	8	32	6.7E-5	-	-	66	3.1E-4	-	-	3.77E-4	0.25
	GaAs	0.5	2.5	-	-	-	-	66	3.1E-4	-	-	3.1E-4	0.2
b	GaAs	2	10	-	-	-	-	66	3.1E-4	-	-	3.1E-4	0.2
	Al <sub>0.6</sub> Ga <sub>0.4</sub> As	2	5.7	111	2.3E-4	-	-	66	3.E-4	-	-	5.4E-4	0.35
	GaAs	100Å	1	-	-	-	-	-	-	3.2	1.5E-5	1.52E-5	0.01
	Al <sub>0.2</sub> Ga <sub>0.8</sub> As	100Å	1	-	-	0.9	1.8E-6	-	-	3.2	1.5E-5	1.7E-5	0.01
	Al <sub>0.6</sub> Ga <sub>0.4</sub> As	2	5.7	111	2.3E-4	-	-	66	3.E-4	-	-	5.4E-4	0.35
	GaAs	0.5	2.5	-	-	-	-	66	3.E-4	-	-	3.1E-4	0.2

Table 3.2 (Part 2) The results of the simulation

structure	material	thickness ( $\mu\text{m}$ )	time (min)	Al1		Al2		Ga1		Ga2		III/H2	growth rate ( $\mu/\text{min}$ )
				sccm	MF	sccm	MF	sccm	MF	sccm	MF		
<b>c</b>	same as <b>b</b>												
	$\Delta\text{Al}_{0.6}\rightarrow 0.2\text{Ga}$	0.2	~13	-	-	5.3 $\rightarrow 0.9$	$1.12\text{E}-5$ $\rightarrow 1.8\text{E}-6$	-	-	3.2	$1.5\text{E}-5$	$2.64\text{E}-5$ $\rightarrow 1.7\text{E}-5$	0.017 $\rightarrow 0.011$
	GaAs	100Å	1	-	-	-	-	-	-	3.2	$1.5\text{E}-5$	$1.52\text{E}-5$	0.01
	same as <b>b</b>												
<b>d-1</b>	$\text{Al}_{0.05}\text{Ga}_{0.95}\text{As}$	5	24	-	-	3.9	$8.1\text{E}-6$	66	$3.1\text{E}-4$	-	-	$3.18\text{E}-4$	0.21
	GaAs	2	10	-	-	-	-	66	$3.1\text{E}-4$	-	-	$3.1\text{E}-4$	0.2
	$\text{Al}_{0.05}\text{Ga}_{0.95}\text{As}$	5	24	-	-	3.9	$8.1\text{E}-6$	66	$3.1\text{E}-4$	-	-	$3.18\text{E}-4$	0.21
<b>d-2</b>	$\text{Al}_{0.05}\text{Ga}_{0.95}\text{As}$	2	9.5	-	-	3.9	$8.1\text{E}-6$	66	$3.1\text{E}-4$	-	-	$3.18\text{E}-4$	0.21
	GaAs	5	25	-	-	-	-	66	$3.1\text{E}-4$	-	-	$3.1\text{E}-4$	0.2
	GaAs	100Å	0.4	-	-	-	-	-	-	8	$3.76\text{E}-5$	$3.76\text{E}-5$	0.0246
	$\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$	100Å	0.33	-	-	3.9	$8.1\text{E}-6$	-	-	8	$3.76\text{E}-5$	$4.57\text{E}-5$	0.03
<b>Max sccm</b>				100		20		100		20			

As = 100sccm  $\approx 10^{-2}$  MF

Zn = 30sccm

Se = 30sccm



compositional changes can be obtained. An instantaneous and precise control of the partial pressures in the reactor system is required for the growth of multilayer structures with abrupt interfaces.

Besides the flow pattern in the reactor system, in the vent and run mode [Ochi86] as shown in Fig3.2, the exact control of vapor pressures in metalorganics(MO) bubblers, precise flow control, zero-dead space in the manifold valve systems and pressure balance for small transient of reactants are all essential for the thickness control and abruptness of the interfaces. As shown in Fig.3.3, when we change, for example, the MO source line from the exhaust line to the reactor line with 100 cc of bubbler volume, 1 Å/sec of growth rate and flow of MO of 5cc/m, 1% of the off-balance pressure can cause 12 Å thickness variation and compositional variation in 1 second in the atmospheric pressure MOCVD system. Therefore precise control of the off-balance pressure and reduction of volume V can be one of solutions for the thickness. Therefore, modification of MO line was done by arranging the mass flow controller as shown in Fig.3.4. In this case volume of the bubbler does not contribute to the transient. Another merit of this location of MFC is to achieve a stable flow rate independent on the outlet pressure, as long as inlet pressure is maintained at twice the outlet pressure. Thus a precise control of the flow can be obtained, once vapor pressures of MO bubblers are maintained constant by use of the precise control of the

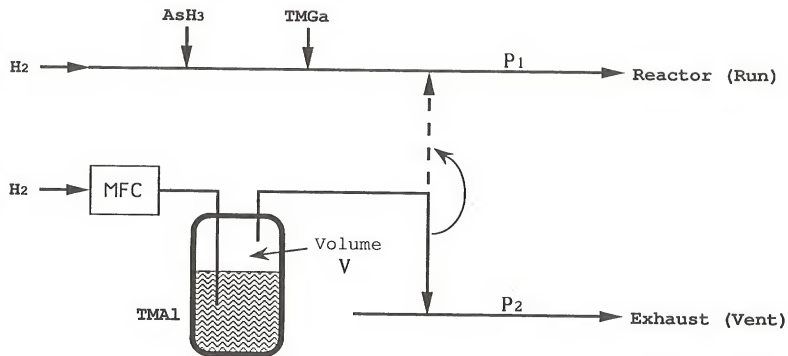


Figure 3.2 Typical vent-and-run mode

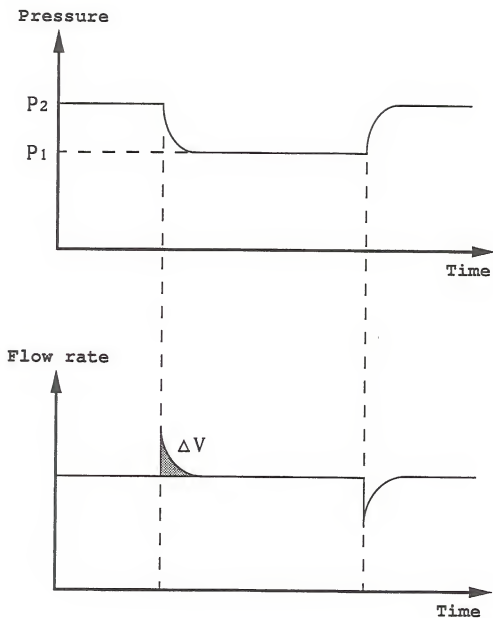


Figure 3.3 Transient response of the flow rate during the switching time from vent to run line;  $P_1$ ,  $P_2$  are the pressures of run-line and vent-line, respectively.

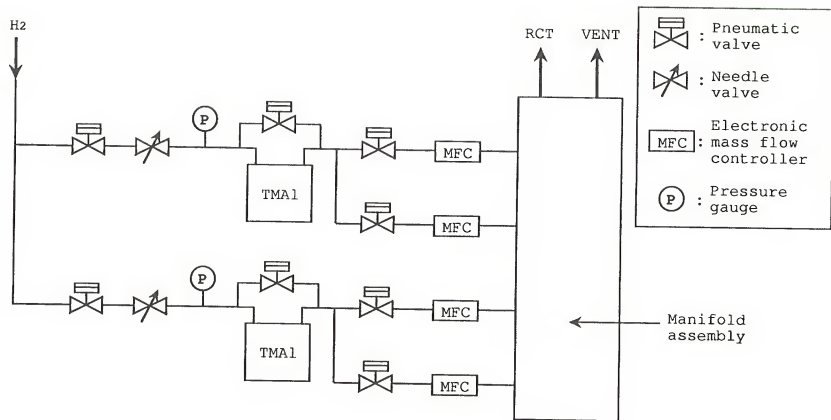


Figure 3.4 Newly-designed metal alkyl bubbler lines

temperatures of MO bubblers. Configuration of two lines also makes it easy to maintain zero pressure difference. Overall gas handling system based on the discussion in the subsections 3.1.2 through 3.1.4 is shown in Fig.3.5.

### 3.1.5 Low defect density

There are many factors which affect the defect density and impurity level; such as purity of sources, leak in the system, cleanliness of reactor assembly, adsorption and outgasing of the surface contaminants, and purification level of the carrier gas, etc. Most of these requirements can be achieved by careful selection of the parts and construction procedure.

In the design, the load-lock chamber system was adapted to prevent the reactor and susceptor from an exposure to uncleaned environments, since most of the  $O_2$  contamination is introduced during the substrate loading and unloading. Reduction of tubing length is also helpful in avoiding the unwanted doping.

## 3.2 Construction and System Description

The designed MOCVD apparatus is grouped into five major subsystems; (i) the gas handling system including the source alkyls (TMGa, TMAI, and DEZn), hydrides ( $AsH_3$ ,  $PH_3$ , and

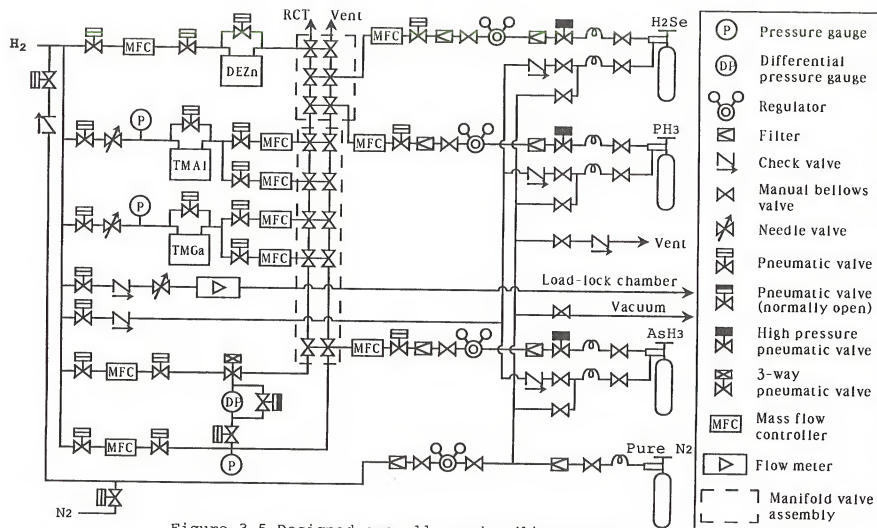


Figure 3.5 Designed overall gas-handling system

H<sub>2</sub>Se), all of the valves, plumbing, and instrument necessary to control the gas flows and mixtures; (ii) the reactor assembly in which the pyrolysis reaction and deposition occur, including the heating system used to obtain pyrolysis temperatures; (iii) the exhaust system to crack the toxic gases( AsH<sub>3</sub>, PH<sub>3</sub> and H<sub>2</sub>Se) which do not participate in the deposition; and (iv) the safety system to prevent the unexpected accidents. Significant attention was given to choosing the parts and the assembly procedure of the system to satisfy the design concepts as well as to achieve the contamination-free system.

### 3.2.1. Gas handling system

To reduce the memory effect which makes difficult to grow the high purity GaAs, fine stainless steel tubing, electropolished up to surface roughness less than 5  $\mu$ inch. RMS and filled with pure N<sub>2</sub> gas by Fujikin, was selected for all the source and carrier gas delivery lines. All the fittings used were VCR fittings and only Neupro stainless steel pneumatic and manual bellows valves were used except for the manifold valve assembly. As a vent-and run inlet manifold assembly for gas-mixing, a 10-valve assembly by Fujikin with zero dead space and fast acting ability ( < 1 sec) was used for TMGa, TMAI, and AsH<sub>3</sub> lines. For DEZn, H<sub>2</sub>Se lines, three-way pneumatic valves by ASM were used. The oil-free check-valves by Fujikin were inserted at critical

positions in the gas handling lines. Automatic welding of the connections was carried out by the Weldlogic welding machine while pure argon(Ar) gas was purging through. Before the welding, each VCR glands and tubings was cleaned by the organic cleaning procedure using the ultra sonic cleaner. The inlet pressures to TMGa and TMAI bubblers are maintained at constant pressures by Modulines' bellow vernier metering valves and monitored via MKS's pressure transducer. Also the differential pressure between the vent line and the run line is monitored and controlled. All the mass flow controllers are electronically controlled by Unit Instruments' products which are able to maintain preset mass flow rate within 0.2 % of accuracy.

Hydrogen gas, purified by a palladium(Pd) diffusion cell which is capable of reducing total impurity levels to less than 0.5 ppm, is used as the carrier gas for TMGa, TMAI, and DEZn. Not shown in Fig.3.6 are two other purifiers connected in series between the H<sub>2</sub> feed gas cylinder and the diffuser. The first of these two purifiers remove O<sub>2</sub> in the feed gas by catalytically combining it with H<sub>2</sub> to form H<sub>2</sub>O which is then removed by a filter in the second purifier. Thus H<sub>2</sub> with less than 1 ppm of O<sub>2</sub> is delivered to the Pd diffuser and this serves to protect and prolong the life of the Pd cell. All purifiers were obtained from Matheson. The moisture range in purified H<sub>2</sub> is monitored via Parametrics' hygrometer and the current dew point reading of -110 °C , which is equivalent to



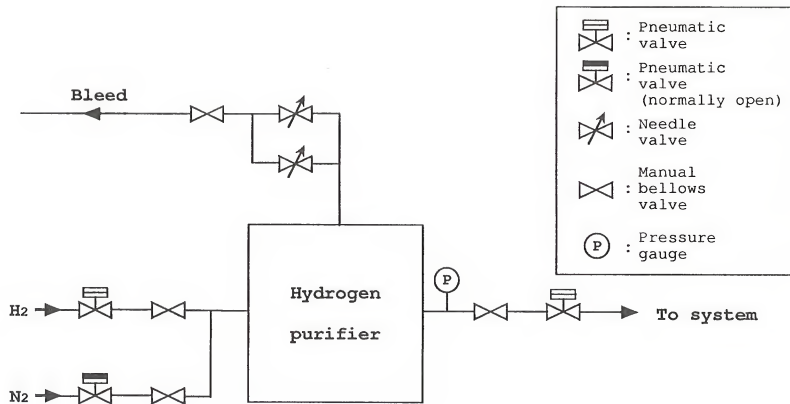


Figure 3.6 Hydrogen purifier assembly

0.001 ppm of moisture, assures the purity of  $H_2$  in the system.

The metalorganics, TMGa, TMA1, and DEZn were purchased from the Alfa Division of Morton Thiokol Inc., with specified purities of 0.01, 0.05, and 0.05 ppm, respectively. They are kept in liquid states inside stainless steel bubblers at specific bath temperature in order to maintain the proper vapor pressure. Controlled accuracies of temperatures of the refrigerated-bath circulators for TMGa, TMA1, and DEZn are within 0.01, 0.1, and 1 °C, respectively. Installed hydride source from Matheson was 99.999 %  $AsH_3$  in a special cylinder whose interior had been treated by ESP (Enhanced Surface Passivation) [Math87] to prevent decomposition of  $AsH_3$  and formation of  $H_2O$ .

### 3.2.2 Reactor assembly

The reactor assembly of our MOCVD system consists of the reactor tube, susceptor, load-lock chamber, vacuum system, and heating system for obtaining the pyrolysis temperature. The first three parts, which are the most important ones, are custom manufactured by Japan Oxygen Inc..

#### Reactor and susceptor

To obtain the uniformity, substantial effort has to be made in proper design of the reactor. Our horizontal air cooled reactor with an inner diameter of 72 mm and a length

of 503 mm (Fig.3.7) is equipped with a special 4-hole sphere at the inlet to spread the gas mixture flow over the entire width of the reactor. SiC coated high purity graphite susceptor with a quartz deflector is tilted at  $15^\circ$  angle into the gas stream in order to prevent formation of a stagnant boundary layer over the wafer that would inhibit the reaction and lower uniformity. The quartz reflector attached to the susceptor is to reduce the geometrical turbulence caused by the front surface of the susceptor. This susceptor is suspended in the central plane of the reactor by one quartz tubing in which a thermocouple is installed for monitoring the susceptor temperature. Reactor tube, deflector, and suspension tube were made of ultra high purity quartz. The reactor and susceptor assembly as shown in Fig.3.7 was tested by the vendor via flow visualization studies to obtain a laminar flow. Before installing the reactor, it was cleaned by use of the following procedure:

- (1) organic cleaning
- (2) Aqua Regia
- (3) HF etching
- (4) Aqua Regia
- (5) Rinse in DI water

#### Load-lock chamber

Load-lock chamber, made of stainless steel with polished inside, was installed in order to prevent the reactor tube and susceptor from an exposure to the contaminated

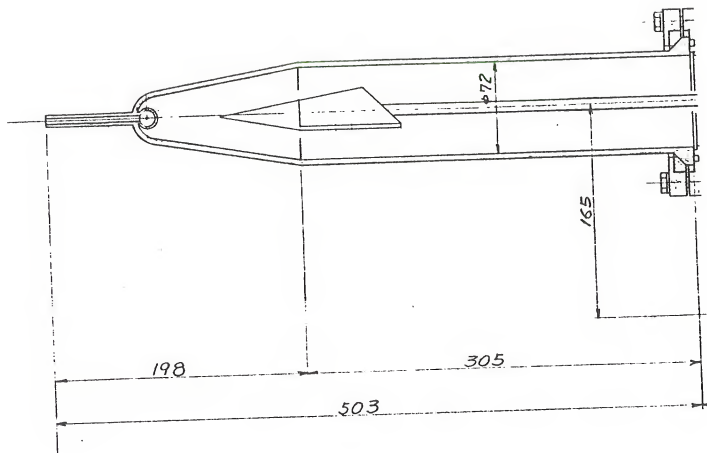


Figure 3.7 Horizontal reactor with susceptor and deflector assembly.

environment during substrate loading and unloading. Substrate loading and unloading is carried out by use of a vacuum tweezer with a quartz tip. Two transparent viewing ports are provided for easy transfer of the substrate and inspection. Moreover, nitrogen atmospheric glove box is used at the entrance of the chamber.

#### Vacuum system

The vacuum system attached to the load-lock chamber is utilized for the evacuation of the chamber, reactor, and gas handling system. Especially, while changing the reactor and sources, a high vacuum is necessary to prevent contamination. It is also used as one of the leak checking methods after changing the reactor. The system consists of a Leybold Heraeus turbo molecular pump with 150 l/min pumping capacity and a mechanical pump.  $1 \times 10^{-6}$  torr of vacuum can be routinely obtained after a two hour pumping time.

#### Heating system

A graphite susceptor is heated inductively via a multi-turn copper load coil fed by a Lepel's radio frequency (RF) induction generator. The RF generator with built-in water-to-water recirculator is controlled automatically by the temperature controller according to the susceptor temperature. Our 7.5 Kw RF generator and temperature controller enable to maintain the preset temperature which ranges from 150 °C to 1000 °C, with an accuracy of  $\leq 1^\circ\text{C}$ .

However, because of the cooling effect of the incoming gases impinging onto the substrate sitting on the susceptor, it is possible that the substrate may actually be at a temperature lower than that of the susceptor. The thermocouple also may detect the slightly lower than actual susceptor temperature due to the lack of direct contact with the susceptor.

### 3.2.3 Exhaust system( Toxic gas scrubber )

After the reactor stage, unused source gases which are toxic and flammable, should be treated properly in the exhaust system for the safety of the environment. Our exhaust system, shown in Fig.3.8, adopts the thermal cracking system since it guarantees economy in system maintenance. The first filter stage filled with glass beads collects all dust particles, which are mostly arsenic powder formed at the end of the reactor by thermal cracking. Filtered toxic source gases are cracked into the solid state and deposited on the walls of the 40-inches long quartz tube, which is heated up to 900 °C by the furnace. Three filtering stages consisting of glass-bead filter, 5  $\mu\text{m}$  fine filter, and the final filter filled with cotton, remove all dust toxic particles produced during the thermal cracking. As the final stage, yellow powder named Mathisol by Matheson, contained in the see-through epoxy-glass container, was used to remove the remaining toxic gases for marginal safety. When this powder reacts with  $\text{AsH}_3$  or  $\text{PH}_3$ , its color changes to white. Final

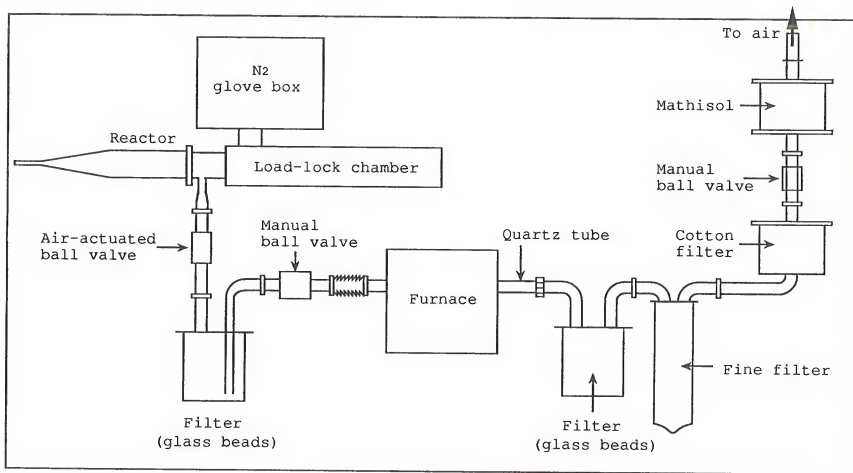


Figure 3.8 Exhaust system

gases coming out of the system are only hydrogen and nitrogen. All the tubings used are 1.5 inches in diameter to prevent blocking of the gas flow. In case of electric power failure during growth, the furnace is backed up by secondary power.

#### 3.2.4 Safety system

The safety system was built for two different purposes. One is to prevent the MOCVD system from contamination due to unexpected reasons such as electric power failure, insufficient water supply, air pressure drop and lack of  $H_2$  and  $N_2$ . The other purpose is to protect the operators from exposure to toxic and explosive gases due to leakage. For the first purpose, various sensors were properly used to monitor the water, air, hydrogen, and nitrogen supplies. For the other purpose, an MDA eight-port toxic gas detector with the sensitivity of 1 ppb and an eight-port  $H_2$  gas detector from Matheson were installed to the home-built automatic alarm system. The functions of this system are listed in Table 3.3.



Table 3.3 Functions of the safety system

	Situation	Operation
Level A	<ul style="list-style-type: none"> <li>• AsH<sub>3</sub> detection(50ppb)</li> <li>• PH<sub>3</sub> detection(50ppb)</li> <li>• Power failure</li> <li>• H<sub>2</sub> detection (20~50ppm) during the night</li> </ul>	<ul style="list-style-type: none"> <li>• Shut off the system automatically</li> <li>• Alarm light</li> <li>• Siren</li> </ul>
Level B	<ul style="list-style-type: none"> <li>• H<sub>2</sub> detection (20~50ppm)</li> <li>• AsH<sub>3</sub> detection(5ppb)</li> <li>• PH<sub>3</sub> detection (5ppb)</li> </ul>	<ul style="list-style-type: none"> <li>• Alarm light</li> <li>• Siren sound</li> </ul>
Level C	<ul style="list-style-type: none"> <li>• Low water flow</li> <li>• Low H<sub>2</sub> pressure</li> <li>• Low N<sub>2</sub> pressure</li> <li>• Failure of H<sub>2</sub> purifier</li> <li>• Low air pressure</li> <li>• H<sub>2</sub> detection (10ppm)</li> </ul>	<ul style="list-style-type: none"> <li>• Warning light</li> <li>• Buzzer sound</li> </ul>

## CHAPTER FOUR

### OPTIMIZATION OF GROWTH PARAMETERS IN THE MOCVD SYSTEM

After finishing the construction of our MOCVD system, a series of characterizations performed to obtain the optimum growth conditions. This chapter describes how to determine the critical growth parameters such as total  $H_2$  flow rate, growth rate, growth temperature, V/III ratio, Al mole fraction. The characterizations, for most grown layers, include measurements of mobility by Hall effect, thickness by Dektak II surface profiler and scanning electron micrograph (SEM), and carrier concentration by Polaron's semiconductor profiler, and photoluminiscence (PL). The surface morphology was studied by the Nomarski optical microscope available in our laboratory.  $GaAs$  and  $Al_xGa_{1-x}As$  epitaxial layers grown on  $GaAs$  substrate under various growth conditions were used for the system characterization.

#### 4.1 Growth Procedure

##### Substrate preparation

For each growth, several pieces (up to 6 pieces) of both n-type and semiinsulating (S.I)  $GaAs$  substrates are prepared from a 2-in. wafer by cleaving it into smaller pieces (typically 1 to 2  $cm^2$  in area). The size of the substrate can

be varied depending on the type of holder installed in the load-lock chamber. In our system substrates up to 6 cm<sup>2</sup> in size can be used. Prior to insertion into the load-lock chamber, substrates are cleaned and etched by use of the following steps:

- (1) Dip in warm trichloroethane(TCE) for 20 minutes;
- (2) Rinse in acetone;
- (3) Rinse in methanol;
- (4) Rinse in deionized(DI) water;
- (5) Etch in  $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 20:7:100$  solution for 2 minutes
- (6) Rinse in DI water
- (7) Blow dry by filtered Nitrogen

As soon as the final step is done, all the substrates were loaded into the load-lock chamber in order to minimize exposure to the air. Together with the GaAs substrate, sometimes Si substrate was loaded for thickness measurement in DektakII surface profiler, after following organic cleaning procedure.

### Growth

After loading the substrates on the graphite susceptor, actual growth steps shown in Fig.4.1 are followed sequentially. In these steps, there are several critical time intervals. Between the first step ( $\text{H}_2$  main flow) and the second step (flow  $\text{AsH}_3$ ), 20 - 30 minutes are required for

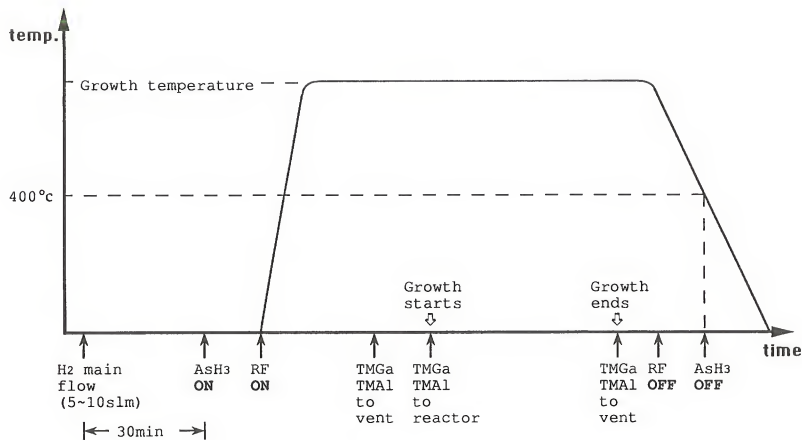


Figure 4.1 Growth sequence for the growth of GaAs

establishing a constant flow rate and pressure inside the reactor. The interval of 15 minutes as a minimum duration between the second step and the fourth step (flow TMGa and TMAI to vent line) is needed to achieve sufficient  $\text{AsH}_3$  partial pressure. Also for the stabilization of the TMGa and TMAI flow, at least 10 minutes are necessary before starting the growth.

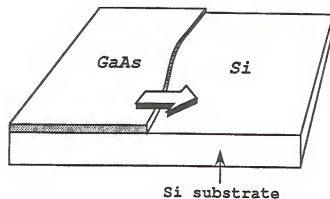
In the cooling procedure after RF is turned off,  $\text{AsH}_3$  flow should be maintained at least up to  $400^\circ\text{C}$  in order to avoid decomposition of GaAs or AlGaAs.

#### 4.2 Methods of Characterization

##### Thickness

DektakII surface profiler was used for the thickness measurement after partly etching the GaAs polycrystalline layer on Si substrate. The schematic figure of the partly etched surface and the profile are shown in Fig4.2, as an example. Also, after growing GaAs and  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  layers alternatively, scanning electron micrograph(SEM) pictures as shown in Fig.4.3 were taken as an alternative thickness measurement method following the A-B etching. The used A-B etchant is a mixture of two solutions. Part A is  $0.3\text{g AgNO}_3 + 40\text{cc H}_2\text{O} + 40\text{cc HF}$  and Part B is  $40\text{g CrO}_3 + 40\text{cc H}_2\text{O}$ . The mixture is PartA:PartB: $\text{H}_2\text{O} = 1:1:1$ .

(a)



(b)

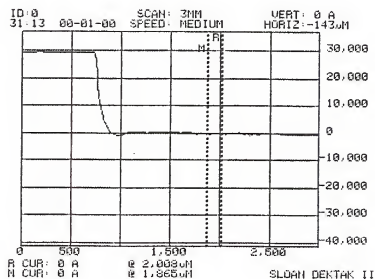


Figure 4.2 Method for the thickness measurement by use of DektakII profiler; (a) etched GaAs on Si ( $\Rightarrow$  is the scanning direction); (b) measured result



Figure 4.3 SEM picture of multilayer structure of GaAs and AlGaAs after A-B etching: thin layers are AlGaAs layers.

### Photoluminescence

PL measurements whose experimental set-up is shown in Fig.4.4 were carried out on most samples at room temperature to check the crystal quality and the Al mole fraction. The PL measurement technique can be utilized for thickness measurement of very thin layers such as quantum wells.

### Carrier concentration

4200 Polaron's semiconductor profiler was used for the doping study and the carrier concentration measurement of the grown epitaxial layers.

### Mobility

The purity of a semiconductor material can be determined by measuring the mobility of the electrons and holes through the crystal lattice of the epitaxial layer. High mobilities indicate that the number of impurities in the semiconductor crystal is low, since electrons are not slowed down by scattering from impurity atoms. Hall mobility measurement was carried out at room temperature. Only the samples grown on semi-insulating GaAs substrates can be used for the measurement. Ohmic contact was made via annealing procedure at 400 °C with a flow of the forming gas (10% H<sub>2</sub> + 90% N<sub>2</sub>). The contact material used was pure indium (In). Measurements were carried out at magnetic field of 0 and 4500 gauss.



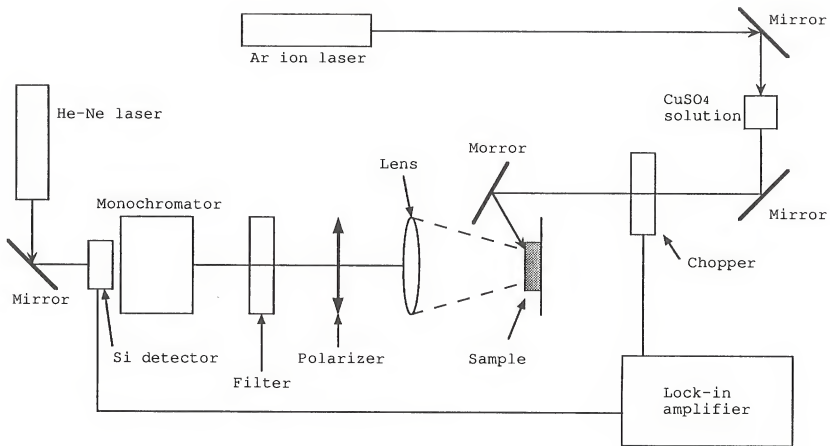


Figure 4.4 Photoluminescence measurement setup at room temperature

### 4.3 Results of Characterizations

In order to arrive at the optimal growth parameters, various growth conditions were studied. Several main H<sub>2</sub> flow rates (5 slm, 8 slm, and 10 slm) were tested for growth of undoped GaAs at growth temperatures of 550 °C, 600 °C, 625 °C, 650 °C, 700 °C, 750 °C, and 800 °C. Several V/III ratios were also tried. Growth time for each GaAs sample was fixed to 30 minutes for the comparison. Various TMGa mole fractions were also used for the growth.

#### 4.3.1 Main H<sub>2</sub> flow rate

At 5 slm flow, the grown surface contains a large number of pits. The growth rate at each H<sub>2</sub> flow rate is given in Fig.4.5. In Fig.4.6, growth rate at 10 slm shows relatively slow changes in the growth rate with the growth temperature. Fig.4.5 shows that the growth at 10 slm is more effective than with other flow rates. The measured mobility and PL spectra showed that the GaAs grown at 10 slm was of the best quality. Therefore 10 slm of H<sub>2</sub> flow rate is the optimal flow rate and is matched to the initial design in our system.

#### 4.3.2 Growth rate

Growth rates at various temperatures and TMGa mole fractions were calibrated. It was observed that the growth rates are linearly increased according to the TMGa mole fraction as shown in Fig.4.7. Fig.4.8 shows the change of

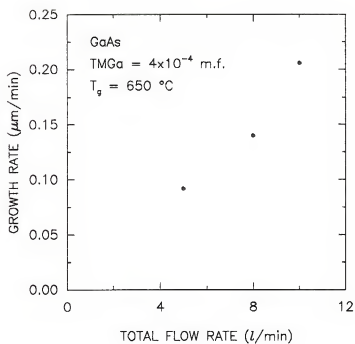


Figure 4.5 the growth rate at different total flow rate.

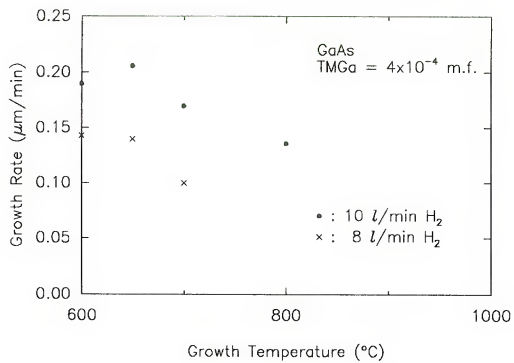


Figure 4.6 Growth rate of GaAs at different growth temperature

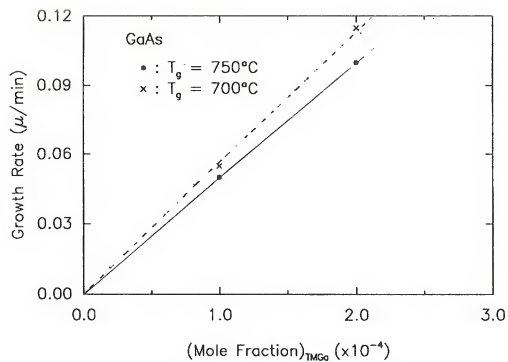


Figure 4.7 Growth rate vs. TMGa mole fraction at 10 slm total  $\text{H}_2$  flow rate.

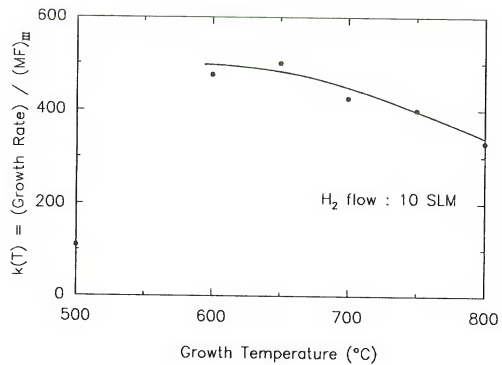


Figure 4.8 Change of the ratio of growth rate and TMGa mole fraction against growth temperature.

growth rate vs. growth temperature. It is relatively independent between 700 °C and 750 °C. The growth rate of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  was slightly larger than that of GaAs at 750 °C, as shown in Fig.4.9.

#### 4.3.3 Growth temperature

Optimal growth temperature had been determined based on the results of PL measurements, surface morphology, the mobility, and the controllability of thickness for GaAs. The best GaAs layer with good surface morphology among the epilayers grown at various temperatures was obtained at 750 °C. The GaAs grown at 750 °C has the highest mobility of  $\mu = 8100 \text{ cm}^2/\text{V}\cdot\text{sec}$  and a low background carrier concentration  $n = 1.4 \times 10^{14} \text{ cm}^{-3}$ , which is comparable to the state-of-the art in MOCVD technology of GaAs. The PL halfwidths at room temperature for GaAs epilayer grown at 750 °C ranged from 28 meV to 35 meV.

#### 4.3.4 V/III ratio dependence

At 10 slm  $\text{H}_2$  flow and growth temperature of 750 °C, the dependence of the carrier concentration has been checked. The carrier concentration increases as the V/III ratio increases as shown in Fig.4.10. However, the changes are small and we could not measure the carrier concentration at  $\text{V/III} = 10$  by Polaron's profiler due to the high resistivity. The mobility as a function of V/III ratio is shown in Fig.4.11. The highest mobility was achieved at  $\text{V/III} = 15$ .

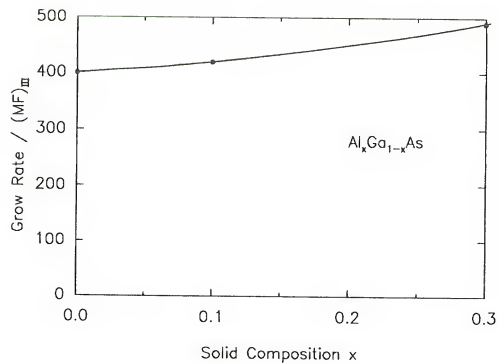


Figure 4.9 Growth rate of AlGaAs vs. Al solid composition  $x$  grown at 750 °C.



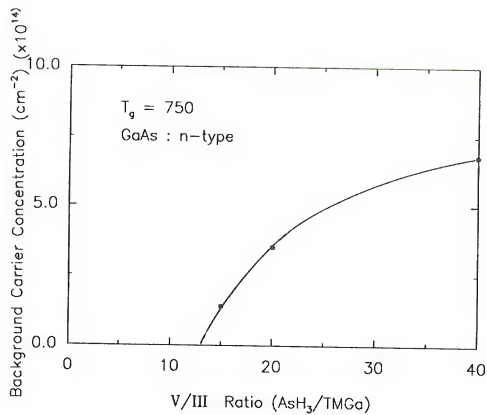


Figure 4.10 Background carrier concentration of undoped GaAs at different  $\text{AsH}_3/\text{TMGa}$  ratios.

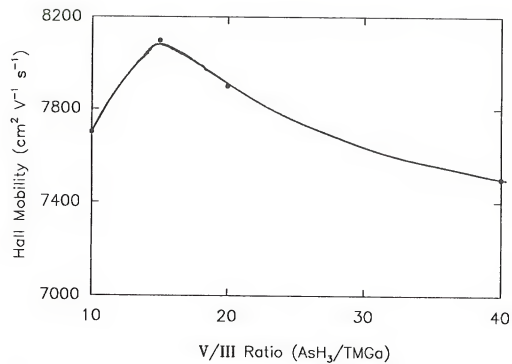


Figure 4.11 Hall mobility of the undoped GaAs layer at different  $\text{AsH}_3/\text{TMGa}$  ratio.

#### 4.3.5 Al mole fraction

Al mole fraction can be determined by the PL measurement by use of the relation between Al mole fraction and PL peak wavelength as shown in Fig.4.12. Our measured peak wavelength of PL spectra of grown samples ( $x = 0.05, 0.1, 0.26$  and  $0.3$ ) are also shown in Fig.4.12. Measured Al solid compositions corresponds to the estimated values of  $x$  with error less than 10 %.

#### 4.3.6 Uniformity

The uniformity of the grown layers was checked by the SEM picture of the multilayered structure shown in Fig.4.3. SEM pictures were taken in an interval of every 1 mm in the direction of the  $H_2$  flow as well as the direction perpendicular to the  $H_2$  flow. As shown in Fig.4.13 and Fig.4.14, in the direction perpendicular to the  $H_2$  flow, the grown layers are fairly uniform except for the edge layers, regardless of the thickness of the layer. However in the direction of the  $H_2$  flow, the grown layers are thinner at the front edge and thicker at the back edge. The variation of the thickness are in the range of  $0.1 \mu m \sim 0.5 \mu m$  over 1 cm length, depending on the thickness of the grown layer.

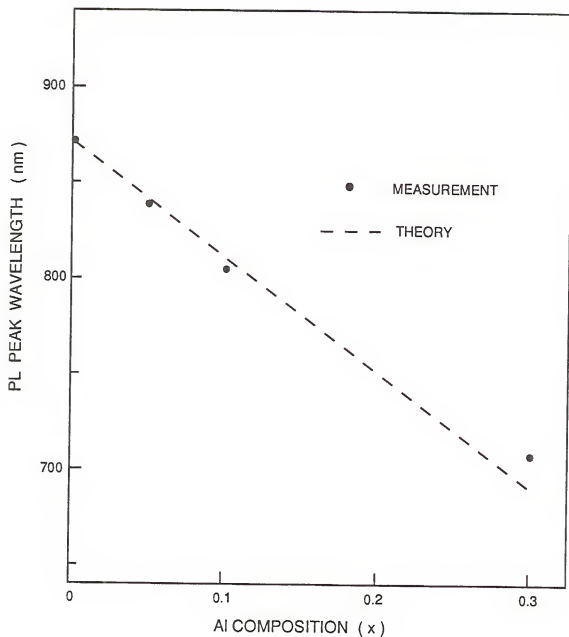


Figure 4.12 Measured PL peak wavelengths vs. Al composition  $x$  for  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ . Solid line represents the relation between energy band gap and solid composition  $x$ .

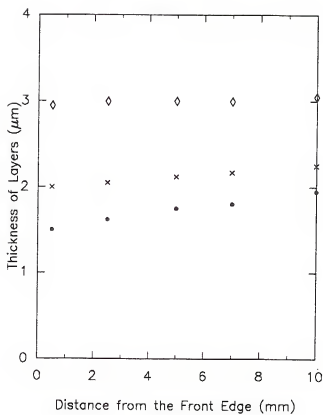


Figure 4.13 Variation of the grown GaAs layer thicknesses along the direction of the H<sub>2</sub> flow.

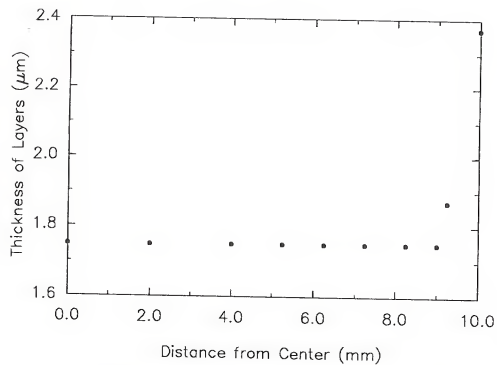


Figure 4.14 Variation of the grown GaAs layer thickness along the direction perpendicular to the  $\text{H}_2$  flow.

## CHAPTER FIVE

### GALLIUM ARSENIDE ON SILICON SUBSTRATE

This chapter describes the properties of GaAs on Si substrate. After explaining the advantages of GaAs-on-Si in the first section, the physical properties of the GaAs-on-Si along with the associated problems will be discussed in the second section. In the third section the growth of GaAs-on-Si by MOCVD and the results of the film characterization will be discussed. In the final section the stress analysis of GaAs-on-Si will be described.

#### 5.1 Advantages of GaAs on Si Substrate

##### Wafer size

GaAs wafers with diameters up to 3 inches are already commercially available. On the other hand, Si wafers are readily available in diameters up to 10 inches. Although GaAs wafers with 3 inch-diameter are adequate for many applications, particularly discrete devices, larger diameter GaAs wafers are ultimately desirable for processing large chips such as LSI (large scale integration) memory or logic with acceptable yields. Especially, monolithic microwave integrate circuits (MMICs), which are inherently large-area chips, should be processed on the largest wafers available.

Unfortunately, it is known that the low thermal conductivity of GaAs imposes fundamental limitations on achieving large diameter wafers without sacrificing crystal imperfection [Jord84]. Therefore, GaAs-on-Si heteroepitaxy could be a solution for processing large chips.

### Cost

GaAs wafers are approximately 25 ~ 30 times more expensive than Si wafers. Therefore, at first glance it would appear that the use of Si substrates would provide substantial cost savings. However, considering the high cost of GaAs epitaxial layers, the cost saving by using a Si substrate instead of GaAs is not so impressive. For most applications significant cost advantages for GaAs-on-Si would be realized only when the technology enables manufacturing cost reductions through the use of substrate sizes larger than are available in GaAs. Significant savings can also be provided by the use of current Si processing equipments. According to the history of Si technology, so many process equipments had been abandoned as the sizes of Si wafers were getting larger (from 2 inches to 10 inches in diameter).

### Wafer strength

Relative to Si, GaAs is a much more fragile material. This is borne out by the experience in implementing GaAs manufacturing activities when one of the major yield loss factors is often simply the wafer breakage in handling. The



problem is magnified by use of larger wafers. On the other hand, Si is known to be 2.5 times more resistant to fracture. Furthermore, process equipment is generally designed to optimally handle Si wafers. Larger-diameter GaAs wafers with density and thickness different from Si would cause handling problems with processing equipments. Thus by depositing GaAs on Si substrate, yield losses due to handling during processing could be significantly reduced.

#### Wafer thermal conductivity

As shown by Fig5.1.[Sze81], the thermal conductivity of Si exceeds that of GaAs by a factor of four over the temperature range of interest for most devices. This can be very advantageous for dissipating heat from high power density devices such as power field effect transistors or lasers. Especially, for the future OEICs, heat dissipation will become a major problem to be overcome. Furthermore, use of Si substrate can allow more desirable device design and mounting configurations due to its larger thermal conductivity. For example, GaAs lasers are usually mounted junction-down onto a heat sink, called 'flip-chip' mounting. For coupling to optical fibers or integration, it is desirable to mount them in the junction-up configuration; however, in this arrangement the substrate becomes the dominant portion of the thermal resistance [Joyc75]. It is calculated that by use of a Si substrate with its higher thermal conductivity, the thermal resistance of the junction-

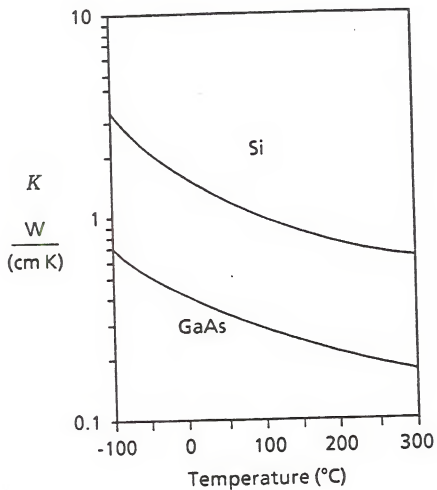


Figure 5.1 Thermal conductivities of GaAs and Si as a function of temperature.

up configuration can be reduced to the point where it is only 16% greater than that of the junction-down configuration on a GaAs substrate [Saka85]. Flip-chip mounting could then be avoided.

#### Wafer density

The lower density of Si in comparison to GaAs can be advantageous for devices for space-based applications such as solar cells.

### 5.2 Problems of GaAs-on-Si and Current Status

#### Native oxide on Si

The very stable native oxide on silicon substrates represents the first barrier to the epitaxial growth of GaAs on Si. This thin oxide layer isolates the underlying ordered Si lattice and exposes an amorphous surface to incoming III-V species. In fact, the native oxide proved to be an effective barrier to earlier attempts to grow the epitaxial GaAs on Si substrate. Various surface preparation techniques have been developed to overcome this problem. Among them, Shiraki method [Ishi86] used mostly in MBE and HF dip method [Akiy84] used in MOCVD, followed by high temperature annealing process are commonly used techniques to achieve the single crystal GaAs epitaxial layers on Si substrate.

Antiphase Domain (APD)

Some GaAs crystal orientations, including the most desirable {100}, consist of alternating monoatomic layers of Ga and As atoms. Unless the Si substrate surface is atomically flat (or all steps are an even number of atomic layers in height) and growth proceeds without two dimensional nucleation, multiple nucleation will occur on the surface; and when these regions grow together to form a continuous film, the layers of a given species may or may not be in alignment with the same species from one separately nucleated region to the other. If the two regions are misaligned, then the resultant boundary, called an antiphase boundary, is formed as shown in Fig.5.2. These defects were commonly encountered in the early films and were once considered to be a major limitation to the technology. The major development of APD free growth was achieved by use of an intentionally misoriented or 'tilted' substrate with a surface orientation of about  $2 \sim 4$  degrees from the (100) toward the [011] direction [Kroe86]. Silicon surface with this orientation is known to be rearranged to form steps with double-atomic-layer heights during high temperature annealing [Saka86a]. Most of the APD free GaAs-on-Si materials are obtained by this technique and schematic cross-section of an APD free GaAs-on-Si is shown in Fig.5.3. However, the step-doubling mechanism and the exact temperature range for step-doubling are yet to be clear. To date, by achieving the APD free GaAs on a nominally (100)-oriented Si substrate after a prolonged high-

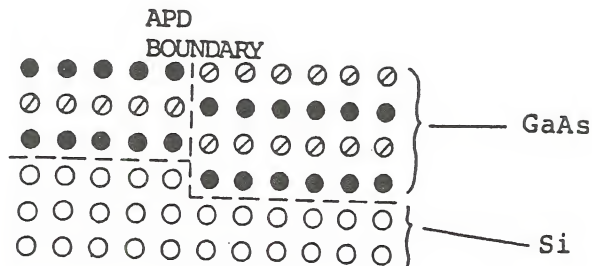


Figure 5.2 Antiphase domain boundary formed on the single step Si surface.

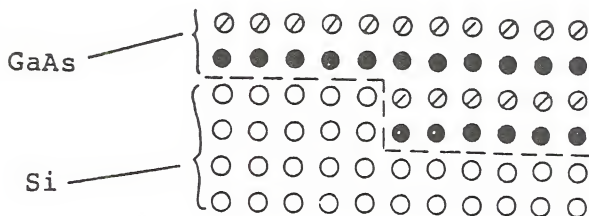


Figure 5.3 APD free GaAs on the double step surface of Si substrate.

temperature anneal [Saka86b, Kawa88, Shas86], APD is no longer a problem for the growth of GaAs on Si substrates.

### Dislocations

The tilted surface orientation serves to significantly reduce another type of crystal imperfection, that is, threading dislocations associated with the lattice mismatch. The 4% difference in the lattice constants for GaAs and Si, if entirely accommodated by misfit dislocations, would result in dislocation density of  $5 \times 10^{11} \text{ cm}^{-2}$ . In practice, the actual density of dislocations that thread into the thicker regions of the epitaxial layer is orders of magnitude lower when the proper growth regime is followed. In the very early stages of growth, the lattice mismatch is accommodated at least partially by compressive strain, and the GaAs lattice spacing contracts in an attempt to match the underlying Si spacing. After the growth of a few nanometers of GaAs, the strain energy exceeds the energy required to form dislocations and misfit dislocations are formed. Two types of misfit dislocations are observed to occur [Otsu86]. One of these lies in the interface plane and does not generate threading dislocations that propagate into the epitaxial layer. Obviously, misfit dislocations are unfavorably developed into the threading dislocations. By use of tilted substrates most of the misfit dislocations are the favorable types that are localized in the interface region. Additional dislocation reduction can occur by several methods, such as buffer

layers( strained superlattice layer or low temperature grown thin GaAs layer) [Saka86, Vern86], *ex-situ* annealing [Lee87, Nish88], and *in-situ* annealing [Choi87]. By use of the above approaches to minimize dislocations and their propagation, GaAs-on-Si structures have a region of poor crystal perfection localized to within 100 ~ 300 nm of the interface. This is followed by the remainder of the epitaxial layer which has a relatively good perfection. The minimum dislocation density achieved up to date is  $10^4 \text{ cm}^{-2}$  [El-M89]. For devices whose critical current paths are located near the upper surface of the epitaxial layer, such as field effect transistors, the imperfect interface is innocuous. However, some potential applications of GaAs-on-Si required carrier transport through the interface region reveal the poor performance of devices. Especially, for the reliable CW operation of lasers at room temperature, a density of dislocations less than  $10^2 \text{ cm}^{-2}$  is necessary.

#### Thermal expansion mismatch

A potentially serious problem in device applications is wafer bowing that results from different thermoelastic properties of GaAs and Si. On cooling from the epitaxial growth temperature, the free contraction of GaAs is 2.5 times greater than that of Si as shown in Table 1.2. The resulting wafer is bowed with a concave GaAs surface and high tensile stress within the GaAs layer as shown in Fig.A.1. Depending on the grown GaAs layer structure such as film thickness and



superlattice intermediate layers, the wafer bow may range from 10  $\mu\text{m}$  to greater than 50  $\mu\text{m}$  over a 2 inch-diameter wafer [Ueda88, Ogas89]. In severe cases, when the tensile stresses exceed the elastic limits of GaAs, cracking occurs. For the fine-line lithography required for LSI circuits, the wafer bow should be less than 10  $\mu\text{m}$  over a 2-in. wafer. It has been known that the extent of wafer bow is dependent on the growth temperature [Vilm82]. However, a recent report shows that the wafer bow is independent of growth temperature above 600  $^{\circ}\text{C}$  and the wafer bow below 10  $\mu\text{m}$  for 4.5  $\mu\text{m}$  thick GaAs layer can be achieved by use of 1 mm thick 2-in. Si substrates [Ueda88]. In addition, other techniques such as growth at the lowest possible growth temperature (below 500  $^{\circ}\text{C}$ ), patterned growth, and insertion of buffer layers with different thermal expansion coefficients [Dupu87, Saka87] have been suggested as solutions for the bowing problem.

### 5.3 Growth of GaAs on Si by MOCVD

#### 5.3.1 Substrate preparation and loading

Nominal (100) Si and Si wafers tilted 2 $^{\circ}$  off from (100) toward [011] were used for the growth. After cleaning the substrates by the organic cleaning method described earlier, the following steps were executed.

Etch in 10:1 BOE etchant for 2 minutes

Rinse in DI water

Dip in  $\text{HF:H}_2\text{O} = 1:2$  for 30 sec

Blow dry with filtered N<sub>2</sub>

Load into the load lock chamber

Evacuate load-lock chamber to 10<sup>-6</sup> torr

Fill the load-lock chamber with H<sub>2</sub> to one ATM.

Load substrates onto the susceptor

#### 5.3.2. Growth

Growth was carried out by use of the two-step direct growth method [Akly84], as shown in Fig.5.4. Annealing at 970°C was done in gas flow of H<sub>2</sub> and AsH<sub>3</sub> for the removal of oxide and formation of double atomic steps. The undoped thin GaAs layers with various thicknesses (200 Å, 500 Å, and 1000 Å) were deposited after the substrates were cooled down to 425 °C. Subsequently, the substrates were reheated to the conventional growth temperature of 750 °C and then 3 μm thick undoped GaAs layers were grown.

#### 5.3.3. Characterization of grown GaAs on Si

The quality of GaAs on different substrates was checked by the Nomarski micrograph and PL measurement. Surface morphology of GaAs on nominal (100) Si shows poor morphology than that on the tilted Si substrate as shown in Fig.5.5. Comparing the PL FWHM in both cases (Fig.5.6), GaAs on the tilted substrate shows better behavior. For the GaAs layers with 200 Å, 500 Å, and 1000 Å of buffer layers, PL show almost same results except for the 1000 Å buffer. Comparison

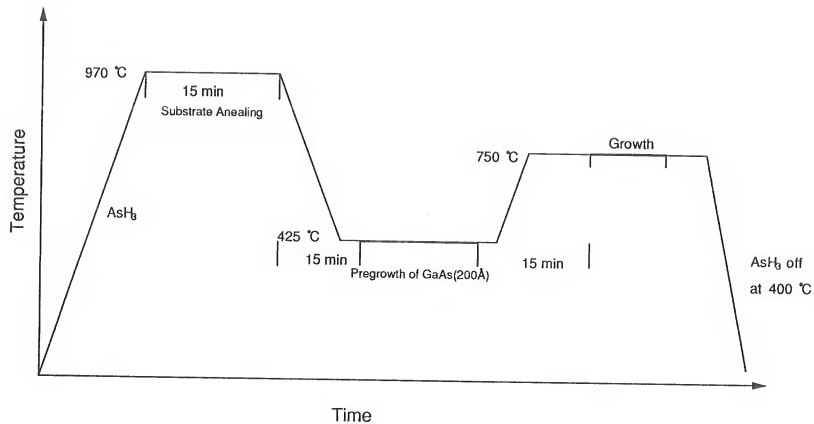


figure 5.4 Growth sequence for GaAs-on-Si.

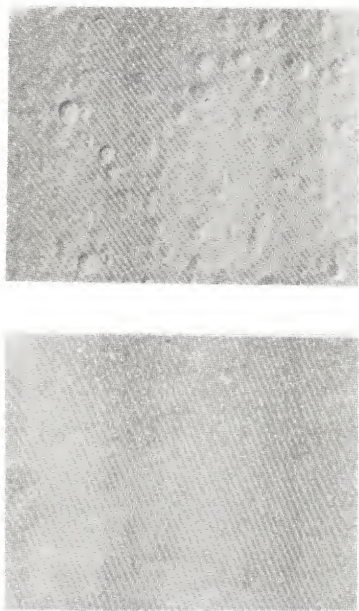


Figure 5.5 Comparison of surface morphology of GaAs grown on nominal (100) Si substrate (top) and  $2^\circ$  off (100) Si substrate (bottom).

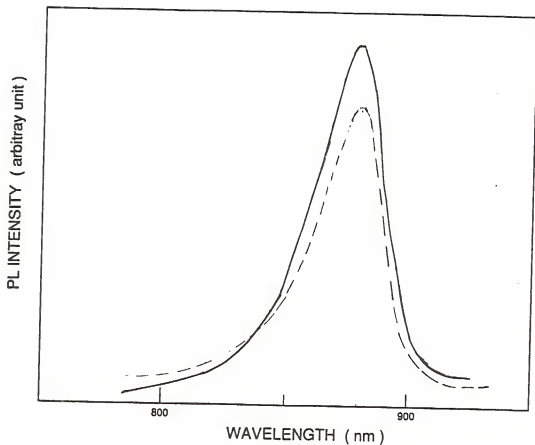


Figure 5.6 Comparison of PL spectra of GaAs grown on nominal (100) Si substrate (dashed line) and 2° off (100) Si substrate (solid line): both spectra show the same peak position at  $\lambda = 883$  nm and almost identical FWHM of 54 meV but different intensities.

of PL spectra between GaAs on Si and that on GaAs in Fig.5.7. show that the peak of GaAs-on-Si shifts toward lower energy, due to the stress in GaAs epitaxial layer which also causes the splitting of heavy hole and light hole band. Moreover, the PL FWHM indicate that GaAs on GaAs is better in crystal quality. Different growth temperatures for the buffer layer were tried. However, grown surfaces were hazy (polycrystal) except for the range from 400 °C to 450 °C and the best mobility was obtained at 425 °C with 200 Å buffer layer. The etch pit pattern etched by molten KOH at 400 °C in Fig 5.8. shows that all pits have a same direction, indicating that the layer has a APD free single domain.

#### 5.4 Analysis and Measurement of Thermal Stress in GaAs-on-Si

Although theoretical stress analysis based on Timoshenko's solution [Olse77, Feng83] and the indirect measurement of stress through the warpage are known [Soga86], the detailed information about interfacial stress distribution of GaAs-on-Si is needed to characterize the thermal stress and to reduce it. We have performed an experiment for the determination of the stress distribution in GaAs-on-Si on the plane perpendicular to the interfacial boundary by measuring stress-induced birefringence [Rein73]. Although GaAs and Si belong to the point group  $\bar{4}3m$  and are optically isotropic [Yari84], GaAs and Si layers in GaAs-on-

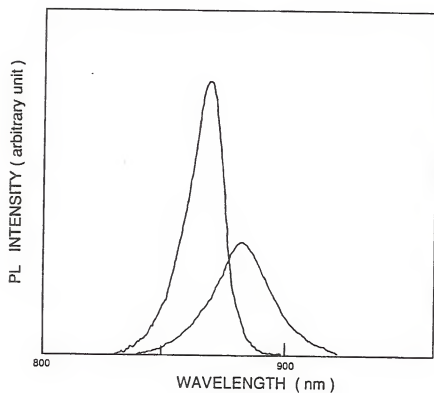


Figure 5.7 Shift of the PL peak of GaAs-on-Si due to the thermal stress. The peak position of GaAs-on-GaAs and GaAs-on-Si are at  $\lambda = 872$  nm and  $\lambda = 883$  nm, respectively.

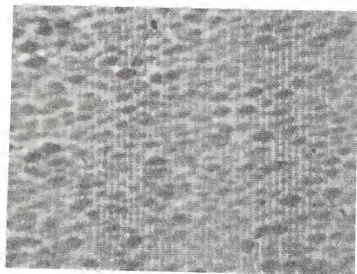


Figure 5.8 Etch pit pattern of GaAs-on-Si etched in molten KOH: every pattern shows same direction.



Si are uniaxial due to the shear stress with the optical axis in the perpendicular direction to the interface. Therefore, the phase retardation between the ordinary and the extraordinary rays can be measured. It is proportional to the stress, if the light propagates in the (100) plane, and is given by [Rein73]:

$$\Gamma = -\pi n^3(p_{11}-p_{12})\sigma L/\lambda$$

, where  $L$  is the light propagation distance parallel to the interface,  $n$  is the refractive index of the material,  $p_{11}$  and  $p_{12}$  are the piezo-optic coefficients,  $\sigma$  is stress and  $\lambda$  is the wavelength of light in free space.

For the experiment, a 2  $\mu\text{m}$  thick GaAs epitaxial layer was grown on (100) Si substrate through two step direct growth method at 650  $^{\circ}\text{C}$ . Growth had been carried out by using the low pressure MOCVD system in the Department of Chemical Engineering. Samples with a thickness of  $\approx 150 \mu\text{m}$ , after lapping the back side, were cut and polished in order to have  $\approx 100 \mu\text{m}$  of light propagation distances. The optical set-up for the measurement is shown in Fig.5.9. A 1.3  $\mu\text{m}$  InGaAsP/InP semiconductor laser was used as a light source and focussed on the sample with its polarization at 45 degrees with respect to the interfacial boundary. The phase retardation measurement was performed by using a Babinet-Soleil compensator. The laser output was end-fire coupled to the front surface of the hetero-boundary and

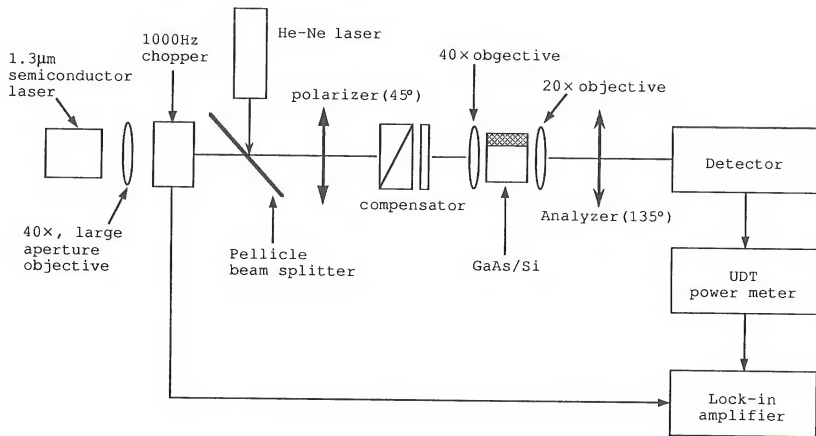


Figure 5.9 Stress measurement setup

scanned along the surface perpendicular to the hetero-boundary.

The sign of the stress induced birefringence was in accordance with the sign of the stress, that is, the stress was tensile in GaAs and compressive in Si. The stress distribution near the interface was not exactly matched to the theoretical distribution because of the relatively large spot size of the beam (25  $\mu\text{m}$ ) compared to the GaAs layer thickness. After the correction of this effect assuming Gaussian beam distribution of the light, the stress distribution is comparable to the theoretical result as shown in Fig. 5.10. The detailed theoretical stress distribution calculation can be found in the Appendix A.

The measured magnitude of stress in GaAs layer was  $0.93 \times 10^9$  dyne/cm<sup>2</sup> which was about one half the theoretical value  $1.8 \times 10^9$  dynes/cm<sup>2</sup>, while Si side near the interface had the value of  $1.1 \times 10^8$  dynes/cm<sup>2</sup> (theoretical value  $1.0 \times 10^8$  dynes/cm<sup>2</sup>).

The measured stress of  $0.93 \times 10^9$  dynes/cm<sup>2</sup> in GaAs layer corresponds to the theoretical value of the GaAs-on-Si grown at 320 °C. Due to high dislocation propagation velocity (.10  $\mu\text{m}/\text{sec}$ ) [Yone87], the dislocations in the GaAs layer move in the large area of the grown layer within the wafer cooling time after the growth. It will be possible that such dislocation motion reduces the stress in the GaAs layer because the dislocations should move to reduce the total energy strain. The above explanation can be strongly backed

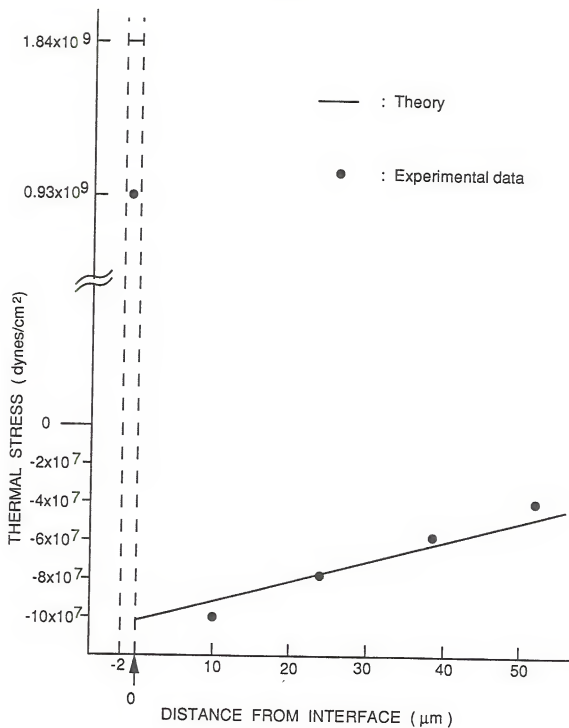


Figure 5.10 The stress distribution of GaAs-on-Si.

in the GaAs layer on Si substrate is independent of the growth temperature [Ueda88] as shown in Fig.5.11. Second, our up by the following experimental evidence. First, the stress measurements of the stress distribution in the dislocation-free Si layer corresponds to the theoretical values. Therefore, to reduce the stress by the low temperature growth, according to above results, GaAs layer must be grown at a temperature less than 320 °C.

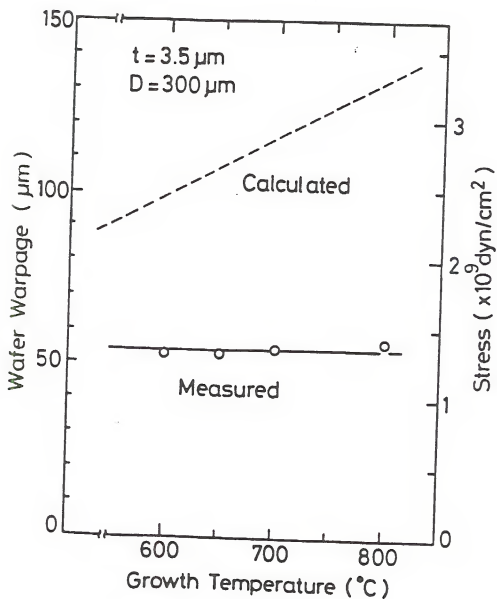


Figure 5.11 Thermal stress of GaAs layer on Si substrate at various grown temperature [Ueda88].

## CHAPTER SIX

### APPLICATIONS OF GaAs-ON-Si TO ELECTROOPTICAL DEVICES

This chapter describes the development of optical waveguides and devices using heteroepitaxial films of AlGaAs and GaAs on Si substrate. In particular, we describe in detail, the fabrication, characterization, and analysis of the waveguides and phase modulators. In the first section, GaAs optical waveguides on Si are discussed. This is followed by the presentation of experimental results of the GaAs phase modulators on both Si and GaAs substrates in the second section; the results are then compared with the theoretical calculations in the final section.

#### 6.1. Optical Waveguides

##### 6.1.1. Design

The thickness of GaAs layer on Si has a limitation due to the induced thermal stress. Usually for thicker GaAs heteroepitaxial layer ( $> 3 \sim 4 \mu\text{m}$ ), cracking occurs permitting the release of stress in the GaAs layer. Therefore, the design of the waveguides was carried out with the constraint that the thickness of total epitaxial layer (guiding and cladding layers) not exceed  $3 \mu\text{m}$ . In fact, the

total thickness was set exactly at 3  $\mu\text{m}$ . In addition to obtain the best quality film possible, the solid composition  $x$  of Al in  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  was kept small. In our devices,  $x = 0.05$ . Refractive indices of 3.420 for GaAs and 3.395 for  $\text{Al}_{0.05}\text{Ga}_{0.95}\text{As}$  at the wavelength of 1.3  $\mu\text{m}$ [Adac85] were used in the theoretical analysis and design. An asymmetric ridge waveguide structure was chosen. The asymmetry helps minimize the interface scattering due to interface roughness. The design emphasized obtaining a well confined single mode for the TE polarization at 1.3  $\mu\text{m}$ . To achieve this, optimizations of the thickness of the guiding and lower cladding layers, and the ridge height were necessary in our simulation as outlined below.

To determine the thickness of GaAs layer, the asymmetric slab waveguide model shown in Fig.6.1. was used. The slab model is only approximate in describing the ridge waveguide structure( Fig.6.10 ). It is only valid for small ridge heights. For 2-D guides, exact analysis is not available. However, number of techniques including effective index method are available to describe the well guided mode. Slab model gives us an indication of the dimensions in the thickness. Thus, we begin with a slab waveguide design. For TE modes, the normalized dispersion relation of waveguide can be written by [Koge74]



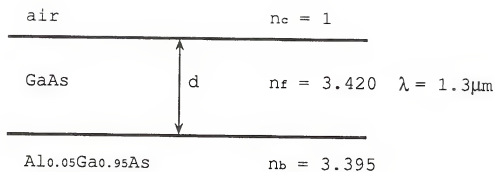


Figure 6.1 Asymmetric slab waveguide configuration

$$V\sqrt{1-b} = m\pi + \tan^{-1} \sqrt{\frac{b}{1-b}} + \tan^{-1} \sqrt{\frac{b+a}{1-b}} \quad (6.1.1)$$

,where  $m$  is the mode number. The normalized frequency  $V$ , the normalized mode index  $b$ , and the asymmetry measure  $a$  are given by

$$V = kd\sqrt{n_f^2 - n_b^2} \quad (6.1.2)$$

$$b = \frac{N^2 - n_b^2}{n_f^2 - n_b^2} \quad (6.1.3)$$

$$a = \frac{n_b^2 - n_c^2}{n_f^2 - n_b^2} \quad (6.1.4)$$

Here,  $n_b$ ,  $n_f$ , and  $n_c$  are the refractive indices of  $\text{Al}_{0.05}\text{Ga}_{0.95}\text{As}$ ,  $\text{GaAs}$ , and air, respectively.  $N$  is the effective mode index defined by

$$N = \frac{\beta}{k} \quad (6.1.5)$$

,where  $\beta$  and  $k$  are the propagation constant of the guided mode and in free space, respectively. At cut off point, we have the mode index  $N = n_b$  and  $b = 0$ . Thus for the guidance of the fundamental( $m = 0$ ) mode only,  $V$  should be in the following range,

$$\tan^{-1} \sqrt{a} < V < \pi + \tan^{-1} \sqrt{a} \quad (6.1.6)$$

Therefore, for the structure shown in Fig.6.1., the thickness of the guiding (GaAs) layer should satisfy

$$0.725 \mu\text{m} < d < 2.299 \mu\text{m}$$

To obtain a well confined single mode, the upper limit of  $d$  is preferred. Thus  $d = 2 \mu\text{m}$  was chosen with a margin. The calculation of the intensity distribution shown in Fig.6.2.(a) indicates that the thickness of  $2 \mu\text{m}$  for the GaAs layer is nearly optimum as observed by the negligible fraction of the power propagating in the substrate.

Possible ridge heights of the waveguide with various widths ( $2 \sim 7 \mu\text{m}$ ) were calculated by use of the effective index method[Rama74], in order to obtain a single mode in the lateral (width) direction resulting in a 2-D single moded ridge waveguide. Calculated results are shown in Table 6.1. As the ridge width increases, maximum ridge height decreases rapidly so that the ridge waveguide is single moded. To avoid the difficulty in etching and to reduce the scattering loss at the etched walls, the width of the ridge waveguide was chosen to be  $6 \mu\text{m}$ . Calculated lateral intensity distribution for the  $6 \mu\text{m}$  ridge is shown in Fig.6.2.(b).

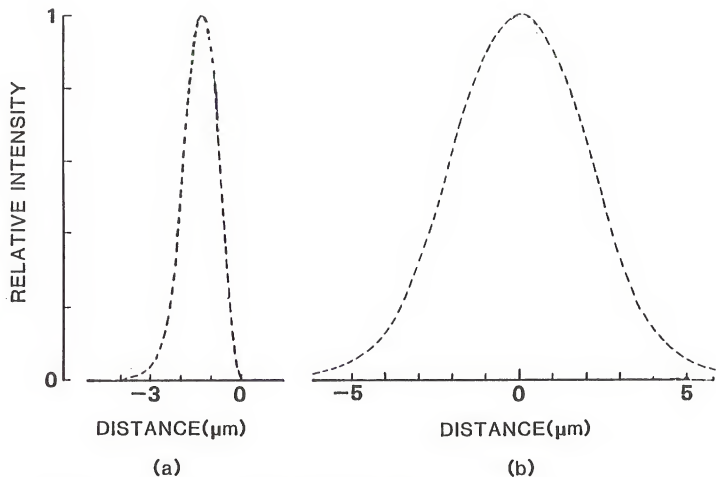


Figure 6.2 Theoretically calculated mode profile: (a) vertical (depth) direction (b) lateral (width) direction

Table 6.1 Maximum etching depth allowed for the lateral single mode in the waveguides with various ridge width

Ridge Width( $\mu\text{m}$ )	Maximum etching depth( $\mu\text{m}$ )
2	1.12
3	0.74
4	0.45
5	0.30
6	0.22
7	0.16

$$n_{\text{GaAs}} = 3.420$$

$$n_{\text{AlGaAs}} = 3.395$$

$$d_{\text{GaAs}} = 2\mu\text{m}$$

### 6.1.2. Fabrication procedure

#### Growth

The first epitaxial layers (sample A) were grown on a high resistivity  $4^\circ$  off (100) Si substrate by MBE at 550 °C using growth conditions discussed elsewhere [Maty87]. It was intended to grow a nominally undoped 1  $\mu\text{m}$  -  $\text{Al}_{0.05}\text{Ga}_{0.95}\text{As}$  cladding layer and 2  $\mu\text{m}$  - GaAs guiding layer sequentially. However, the grown MBE layers were p-type and the carrier concentrations of guiding and cladding layers were  $1.2 \times 10^{17}$  and  $2.2 \times 10^{15} \text{ cm}^{-3}$ , respectively. Carrier concentration profile measured by the Polaron's semiconductor profiler is shown in Fig.6.3. This abnormal high carrier concentration was found to have arisen from an unintentional Be background in the MBE system.

The second sample (sample B) with the same structure grown on a  $4^\circ$  off (100)  $n^+$  Si substrate was also grown by MBE using the same growth conditions. In this case, the carrier concentrations in the undoped guiding and cladding layers were found to be less than  $10^{15} \text{ cm}^{-3}$  as shown in Fig.6.4. The measured carriers were p-type. The surface morphology as measured by Nomarski interference microscope and the micrograph is shown in Fig.6.5. It is typical for the MBE grown GaAs-on-Si.

Both the samples were grown at Central Research Laboratories, Texas Instruments, Dallas, Texas and supplied by Dr. Shichijo's group. The measured oval defect density reportedly was about  $10^2 \text{ cm}^{-2}$ .

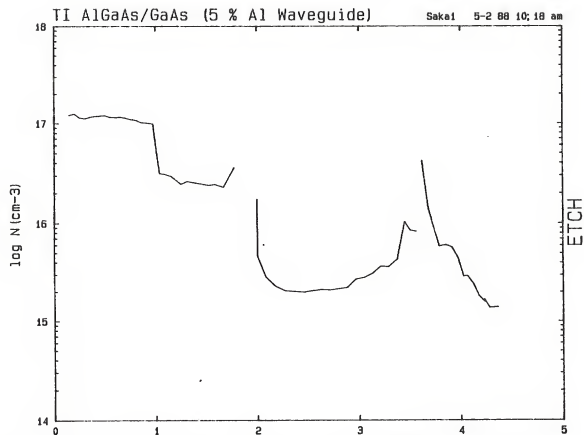


Figure 6.3 Carrier concentration for sample A grown by MBE.

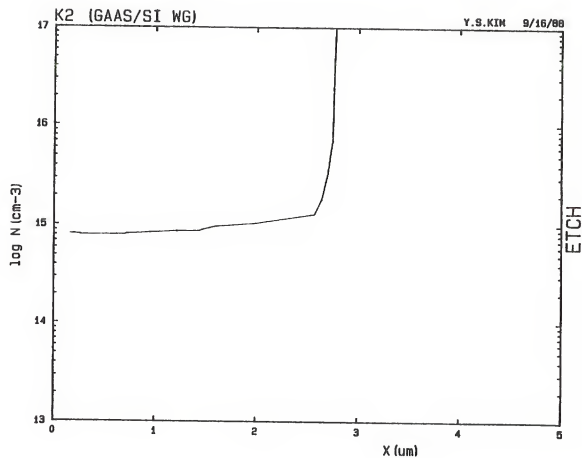


Figure 6.4 Carrier concentration for sample B grown by MBE.





Figure 6.5 Surface morphology of GaAs grown by MBE on Si substrate (sample B).

### Photolithography

Metal masks with various widths ranging from 6  $\mu\text{m}$  to 10  $\mu\text{m}$  with an interval of 0.5  $\mu\text{m}$ , were used for defining the ridge waveguide patterns. For obtaining the best definition, various combinations of UV exposure time and developing time were tried. The processing steps prior to the etching are described as follows:

- (1) Clean in warm TCE for 10 min.
- (2) Rinse in acetone
- (3) Rinse in methanol
- (4) Rinse in DI water
- (5) Blow dry with  $\text{N}_2$
- (6) Bake at 150 ~ 200  $^{\circ}\text{C}$  for 30 min.
- (7) Coat photoresist (Shipley AZ1400 - 17) at 4500 rpm  
at 4500 rpm ( 30 sec.)
- (8) Soft bake at 90 ~ 95  $^{\circ}\text{C}$  for 30 min.
- (9) Expose in UV light for 8 sec.
- (10) Develop with Shipley 351 developer:H $2\text{O}$  = 1:5
- (11) Rinse in DI water
- (12) Hard bake at 125  $^{\circ}\text{C}$  for 30 min.
- (13) Etch

### Etching

Since our ridge waveguide structure requires very small etching depth as shown in Table 6.1, an etchant with very slow etching rate is preferred. This would also yield fine-

etched walls which reduce the propagation losses. For slow etching,  $\text{NH}_4\text{OH}$  - based etchant was tried at various temperatures. Etched depths and roughness of the etched walls were checked by the Dektak II surface profiler and SEM pictures, respectively.  $\text{NH}_4\text{OH}$  - based etchant has slow etching rate (  $0.6 \mu\text{m}/\text{min}$  ) at  $4^\circ\text{C}$ . The compositional ratio of the  $\text{NH}_4\text{OH}$  - based etchant was  $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 20:7:100$ .

#### Facet fabrication

Since the directions of cleavage for GaAs and Si are different - (GaAs has a {110} cleavage directions, while Si has [111] direction) - it is very hard to obtain mirror-like cleavage for the waveguide end surfaces. For mirror-like facets shown in Fig.6.6, the following steps were used;

- (1) Reduce sample(device) thickness to  $50 \sim 60 \mu\text{m}$  by lapping with  $5 \mu\text{m}$   $\text{Al}_2\text{O}_3$  powder
- (2) Polish the Si substrate side with  $1 \mu\text{m}$  diamond paste to obtain the thickness of  $\sim 35 \mu\text{m}$
- (3) Cleave the sample at the Si surface.

#### 6.1.3 Characterization method

Waveguides were characterized at  $1.3 \mu\text{m}$  wavelength using a semiconductor laser as the light source. Fig.6.7 shows the experimental arrangement. To measure the near field intensity pattern and the loss, end fire coupling technique using a single mode fiber was employed rather than a lens with a

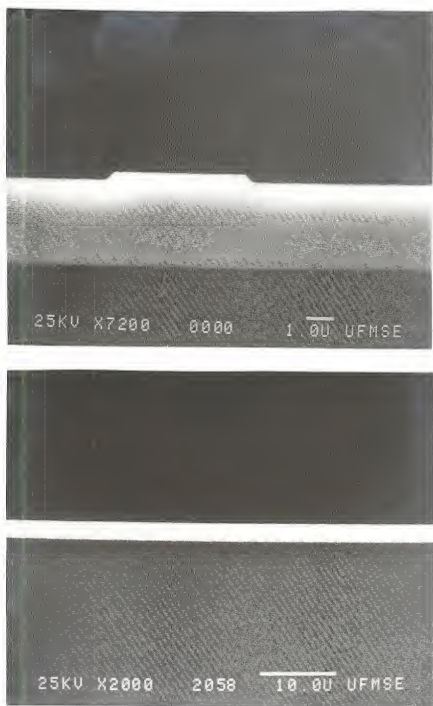


Figure 6.6 SEM picture of fabricated mirror-like end facets of GaAs-on-Si; bright areas are the AlGaAs /GaAs facets.

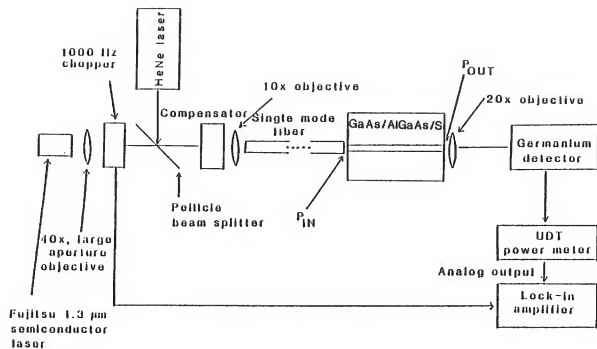


Figure 6.7 Characterization set-up for near field intensity and loss measurements of waveguides.

smaller beam spot size. The TE-like or TM-like linear polarization of input light was obtained by adjusting the Babinet-Soleil compensator at the fiber input. To minimize any possible error caused by different facet reflectivities in the measured losses, every facet was checked carefully through an optical microscope for damages and the presence of any foreign substance. Efforts were made (by positioning the waveguides) to maintain the same level of coupling mismatch between the optical fiber end and the waveguide facet in each measurement. This was achieved by maximizing the guide output. This condition corresponds to maximum transmission through the Fabry-Perot resonant structure formed by the exciting fiber and the waveguide input end. In other words, the Fabry-Perot effect caused by the Fresnel reflections was used by selecting the proper axial spacing (an odd integer multiple of  $\lambda/4$ ) for maximum transmission between the fiber and the waveguide. The waveguide output was collected by a long working distance, high quality planar x20 objective which images the guided mode field onto a Ge photodetector. The two dimensional near field intensity patterns (at a magnification of 65 times) of the guided modes were measured by scanning the detector horizontally and vertically using a 25  $\mu\text{m}$  pinhole and recording the signal from the lock-in amplifier onto the chart recorder. For total power output measurements, the pinhole was removed.

#### 6.1.4 Results

##### Sample A (relatively highly doped GaAs-on-Si)

The waveguide structure of sample A with 6  $\mu\text{m}$  width and 0.25  $\mu\text{m}$  etching depth was fabricated and characterized. The measured near field pattern for TE(Fig.6.8) shows the mode to be well guided and the guide is single moded both in vertical (depth) and lateral (width) direction. The theoretical intensity profile obtained by the effective index approach is also shown in Fig.6.8 for comparison. The measured vertical pattern is somewhat broader (2.2  $\mu\text{m}$  1/e intensity), while the lateral pattern is narrower (4.2  $\mu\text{m}$  1/e intensity) than the theoretically calculated intensity profiles (1.6  $\mu\text{m}$  and 5.5  $\mu\text{m}$  1/e intensity for vertical and lateral patterns, respectively). The measured relative transmissions without the pinhole for the TE mode are plotted against the waveguide length in Fig.6.9. The measured average propagation loss is 11.7 dB/cm for this 6  $\mu\text{m}$  ridge waveguide. This large attenuation is discussed in the next subsection.

##### Sample B ( low doped GaAs-on-Si)

Ridge waveguides of widths ranging from 6  $\mu\text{m}$  to 10  $\mu\text{m}$  in steps of 0.5  $\mu\text{m}$  were characterized. Schematic cross section and SEM picture are shown in Fig.6.10. The near field intensity patterns were measured for both TE and TM polarization. The measured near field intensity profiles show that the guides are single moded and are well confined both

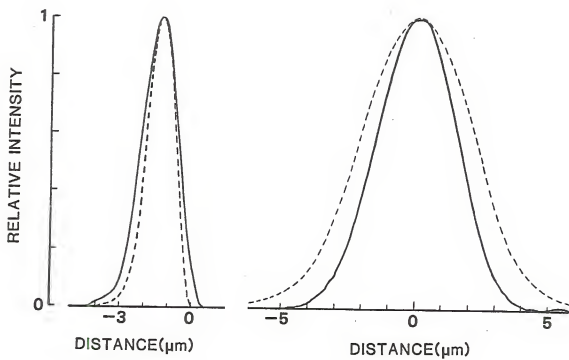


Figure 6.8 Comparison of the measured mode profiles( solid line) with the calculated profiles( dashed line ); vertical direction(left) and lateral direction(right).



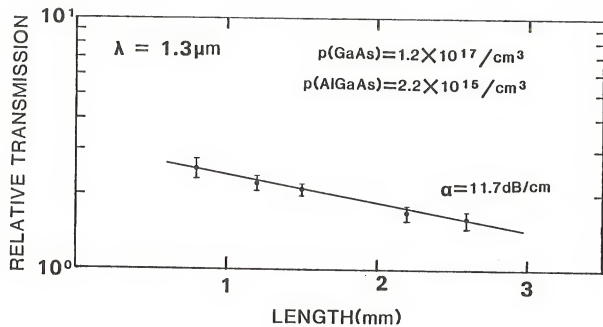


Figure 6.9 Relative transmission vs. length for the fundamental TE mode for sample A.

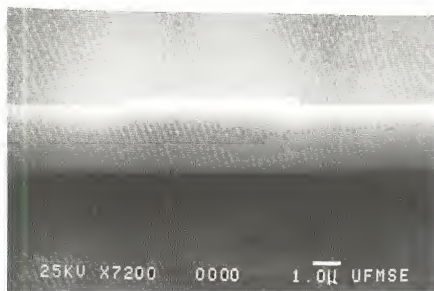
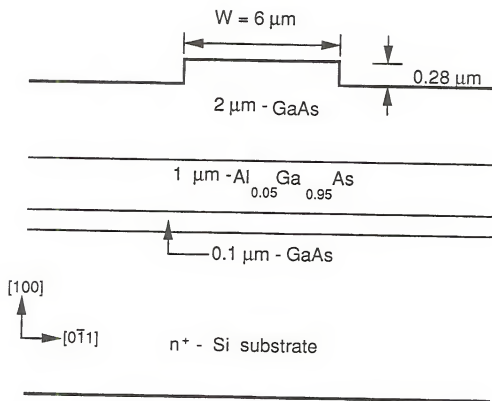


Figure 6.10 Schematic cross section and SEM picture of the GaAs/AlGaAs ridge waveguide on Si substrate.

in vertical and lateral directions even for the 10  $\mu\text{m}$  wide waveguide. The lateral width at  $1/e$  intensity of the near field pattern for a 10  $\mu\text{m}$  wide waveguide was only 0.25  $\mu\text{m}$  wider than for a 6  $\mu\text{m}$  waveguide. The modal width of the TM mode was slightly larger than that of the corresponding TE mode. For instance, as shown in Fig.6.11, for 6  $\mu\text{m}$  waveguide the lateral and vertical differences in the width (at  $1/e$  intensity) between the TM and TE modes are 0.25  $\mu\text{m}$  and 0.2  $\mu\text{m}$ , respectively. There was no measurable difference in mode size for 6  $\mu\text{m}$  wide waveguide between the two samples. This means that the difference in the etching depths (0.03  $\mu\text{m}$ ) in the two samples is not detectable. The measured relative transmission of the waveguide with widths of 6, 6.5, and 7  $\mu\text{m}$  are plotted against the waveguide length for the TE polarization in Fig.6.12. Each data point represent the average of at least two measurements. The error, mainly due to power fluctuation of the semiconductor laser, is less than  $\pm 0.05$  dB. For the TE mode, average propagation losses were obtained by fitting the data points using the least square error method. Propagation losses for 6  $\mu\text{m}$ , 6.5  $\mu\text{m}$ , and 7  $\mu\text{m}$  waveguides were 1.24 dB/cm, 1.20 dB/cm, and 0.95 dB/cm, respectively. Although the lowest value of 0.95 dB/cm was obtained for the 7  $\mu\text{m}$  waveguide by curve fitting, it appears that an average value of 1.20 dB/cm is more reasonable for the GaAs waveguides on Si substrates.

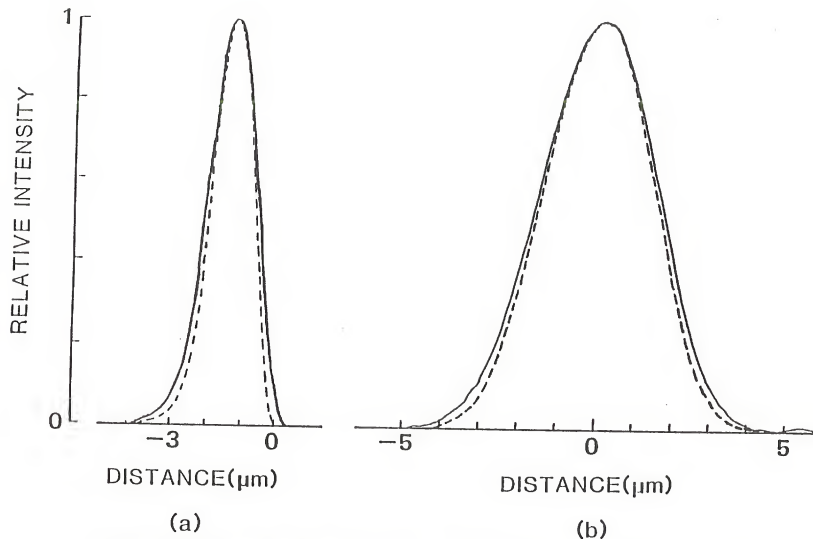


Figure 6.11 Measured near-field intensity profiles of  $w = 6\mu\text{m}$  waveguide. Solid and dashed line represent TM and TE polarization: (a) vertical direction (b) lateral direction.

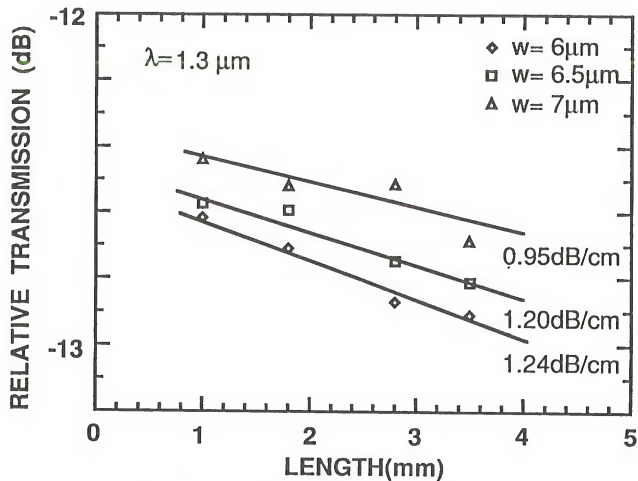


Figure 6.12 Transmission vs. length for waveguides of  $w = 6, 6.5$ , and  $7 \mu\text{m}$  for the fundamental TE modes. Average propagation loss at  $1.3 \mu\text{m}$  are shown by slopes of straight lines.

### 6.1.5 Discussion of waveguide losses

According to the measurement of the first sample, the propagation loss ( $0.7 \sim 3.1$  dB/cm) was estimated theoretically by subtracting the estimated absorption loss of  $9.8 \pm 1.2$  dB/cm (due to high p-type free carrier concentration [Brau59, Case75]) from the measured propagation loss of 11.7 dB/cm. The propagation losses of the second samples are well within the range of the estimated values. The loss in these waveguides (low doped) arises from the free carrier absorption in the substrate, since the tails of the fundamental mode extends slightly into the substrate as shown in Fig.6.2. According to the theoretical model for the slab waveguide calculation [Inou85], our present structure of GaAs waveguiding layer (thickness =  $2 \mu\text{m}$ ) and  $\text{Al}_{0.05}\text{Ga}_{0.95}\text{As}$  cladding layer (thickness =  $1 \mu\text{m}$ ) on an n+ substrate should exhibit a loss of  $\approx 1$  dB/cm for the fundamental TE mode. This implies that, by increasing the cladding layer thickness or the guiding layer thickness, the propagation loss can be further reduced. For example, further reduction in loss of approximately  $0.4 \sim 0.5$  dB/cm can be expected by increasing either cladding layer thickness or the guiding layer thickness by  $1 \mu\text{m}$ . Additional losses come from scattering at the surface, interface, and ridge walls. Consideration of the above mentioned loss mechanism as well as the measured low loss (1.2 dB/cm) in our GaAs waveguide on Si substrate, implies that the presence of a high density of dislocations

(about  $10^8 \text{ cm}^{-2}$ ) in the GaAs layer on Si does not significantly affect the loss of the waveguide.

## 6.2. Phase Modulators

### 6.2.1 The p-N abrupt junction phase modulator on Si

#### Fabrication

To investigate the performance of an optical phase modulator, a phase modulator was fabricated by using the sample B shown in Fig.6.10. Initially, it was our intention to fabricate a Schottky barrier phase modulator. However, what actually we ended up with is a back-to-back diode configuration, as shown in Fig.6.13, due to the p-type low doped GaAs layer. As a result, one sided abrupt p-N junction exists near the GaAs-Si interface. For the modulator, an  $\text{SiO}_2$  insulation layer was deposited on the top surface except over the openings on the top of ridges before the Cr/Au contacts were evaporated. The deposited thicknesses of Cr and Au were 100 Å and 2000 Å, respectively. Cr was used for improving the stickness. After lapping the Si back side to approximately 30 ~ 40  $\mu\text{m}$ , Al was evaporated as the back side contact. The depositions of Cr/Au and Al were carried out by the electron beam evaporator. Typical lengths of modulators ranged from 1 mm to 2 mm after cleaving.

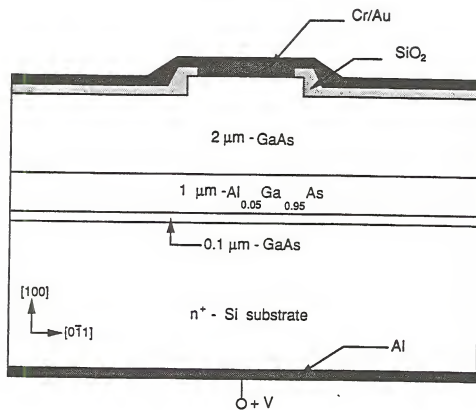


Figure 6.13 Schematic cross section of the AlGaAs phase modulator on Si substrate.



### Measurement

The measured reverse bias breakdown voltages of the device were 6.5 V for GaAs/Si p-N junction and 4 V for Schottky barrier. The Mach-Zehnder interferometer setup shown in Fig.6.14 was used for the phase shift measurement. In order to minimize the drift of the fringe pattern due to the vibration of the pellicle beam splitter in the ambient air movement or pressure variations, the entire setup was enclosed in a box. The optical source used was an InGaAsP laser at 1.3  $\mu\text{m}$  wavelength. The lenses for the input and output of the sample were high quality x40 and x10 UD objectives, respectively. Babinet-Soleil compensator was used for adjusting the optical path difference in order to obtain better fringe contrast. The interference fringe pattern was observed on a TV monitor via an infrared vidicon. By an oscilloscope, proper horizontal TV line(center of the mode) was selected among a series of frames sent by the frame synchronizer which was connected to the TV monitor. With reverse bias of up to 4 V applied to the Schottky barrier, no observable phase shift was seen prior to the break-down. A reverse bias was then applied to the p-N abrupt junction in the opposite direction. For 6 V reverse bias voltage, noticeable shift of fringe pattern was observed. The observed interference fringe patterns with and without reverse bias ( $V_a = -6$  V) are shown in Fig.6.15. For a 1.65 mm long modulator, 36° of phase shift at 6V reverse bias for the pN-junction was obtained for the TE mode and no phase shift

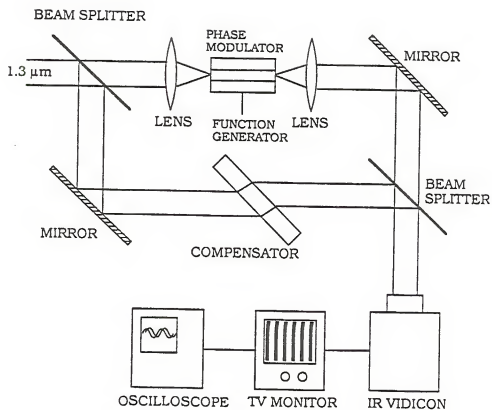


Figure 6.14 Mach-Zehnder interferometer set-up.

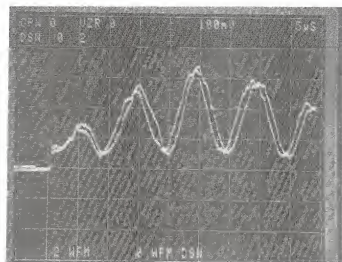


Figure 6.15 Line-scanned interference fringe patterns with and without reverse bias of 6 V.

for the TM polarization was observable ( the shift of less than  $8^\circ$  could not be resolved). These results imply that the phase shift was entirely due to the linear electro-optic effect [Fais87]. The normalized phase shift efficiency is  $3.5^\circ/\text{V}\cdot\text{mm}$ .

#### 6.2.2 Schottky barrier phase modulator on Si

##### Fabrication

Our newly built atmospheric pressure MOCVD system was used for fabricating the modulator structure. Growth was carried out according to the sequences explained in Sec.5.3. An undoped  $0.2\ \mu\text{m}$  - GaAs,  $1.5\ \mu\text{m}$  -  $\text{Al}_{0.05}\text{Ga}_{0.95}\text{As}$  cladding layer, and  $2\ \mu\text{m}$  - GaAs guiding layer were grown sequentially on  $2^\circ$  off (100) n-type Si substrate, after the GaAs nucleation step at  $400^\circ\text{C}$ . Normally the grown layers were n-type and background carrier concentrations in the GaAs guiding layer and the AlGaAs cladding layer were found to be  $9.0 \times 10^{14}$  and  $8.4 \times 10^{15}\ \text{cm}^{-3}$ , respectively, as shown in Fig.6.16. The detailed fabrication procedure is the same as that described in subsection 6.2.1. The schematic structure of the Schottky barrier phase modulator and the crystallographic directions are shown in Fig.6.17.

##### Measurement and result

The reverse biased breakdown voltage of the Schottky barrier was measured through the current-voltage

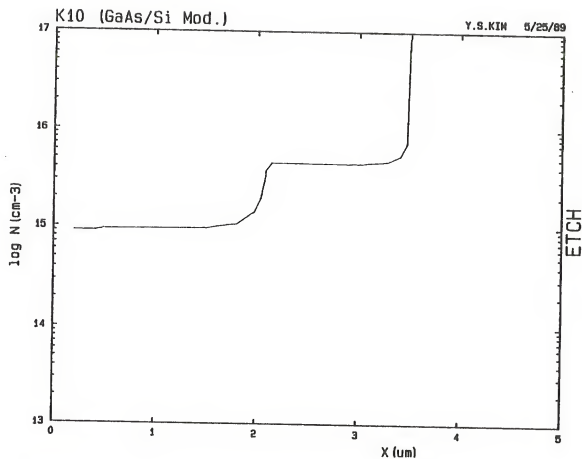


Figure 6.16 Background carrier concentration in the AlGaAs/GaAs layer of the phase modulator structure grown by MOCVD on Si.

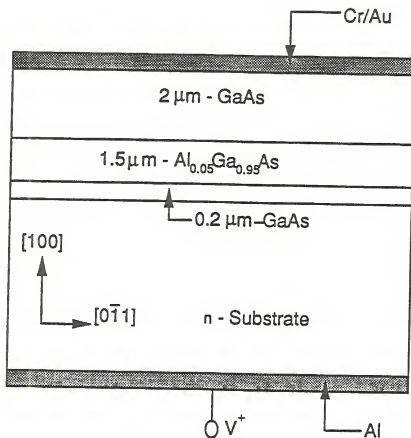


Figure 6.17 Schematic cross section of the planar Schottky barrier phase modulator.

characteristics as shown in Fig.6.18. The same Mach-Zehnder interferometer setup discussed in subsection 6.2.1. was used to measure the phase shift under 4V of the reverse bias. Measurements were carried out for both TM and TE polarization. No observable phase shift was obtained for the TM polarization. In the case of TE polarization, 28° of phase shift was obtained for a 1.5 mm long modulator. The observed line-scanned interference fringe patterns with and without 4V of the reverse bias are shown in Fig.6.19. The above results indicate that the phase shift is primarily due to the linear electro-optic (LEO) effect. The measured phase shift efficiency of 4.7 °/V·mm for the modulator grown by MOCVD is somewhat larger than that of the p-N junction phase modulator.

### 6.2.3 Schottky barrier phase modulator on GaAs substrate

#### Fabrication

For comparison purposes, the Schottky barrier phase modulator with the same structure (except for a buffer layer) was grown on n<sup>+</sup>-GaAs substrate by MOCVD at 750 °C. Considering the cross-doping effect between GaAs and Si, omission of 0.2 μm GaAs buffer layer has negligible effect on the phase shift. The grown layer was n-type and background carrier concentrations in the GaAs and AlGaAs layers were 6.5x10<sup>14</sup> and 1.5x10<sup>15</sup> cm<sup>-3</sup>, respectively. The fabrication procedures are same as that on the Si substrates except the

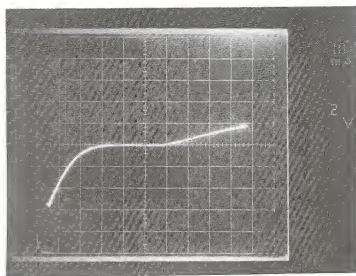


Figure 6.18 Current-voltage trace of Schottky barrier phase modulator on Si grown by MOCVD.



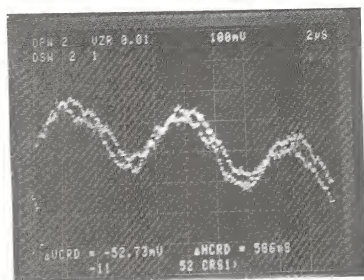


Figure 6.19 Observed interference fringe patterns with and without reverse bias.

lapping and the evaporation of the back side ohmic contact. For backside contact, Au-Ge/Ni/Au was deposited by the E-beam evaporator. After metal evaporation, thermal annealing was carried out at 450 °C for 2 minutes in H<sub>2</sub>-N<sub>2</sub> (5~95%) forming gas ambient. Before the evaporation for back side contact, the substrate side was lapped down to approximately 4 mils to obtain mirror-like facets after cleaving.

### Measurement

Phase shift measurements were performed on two samples with different waveguide lengths (1.99mm and 3.55mm) by using the same set-up except replacing pellicle beam splitter to plate beam splitter. By this replacement, very stable fringe pattern could be obtained. As before, break-down voltage were measured for each sample. As shown in Fig 6.20, breakdown voltages were 20 and 10 volt for 1.99mm and 3.55mm samples, respectively. Fig. 6.21 shows the shift of the fringe patterns of the TE mode in a sample with L=1.99mm as the reverse bias voltage is increased from 0 to 14 V in 2 V steps. No observable phase shift was obtained for the TM mode for upto 14 volts bias.

## 6.3. Analysis of phase shift

### 6.3.1 Phase shift of propagating mode

Starting from the one dimensional scalar wave equation (Helmholtz equation) for three layer slab waveguide, the

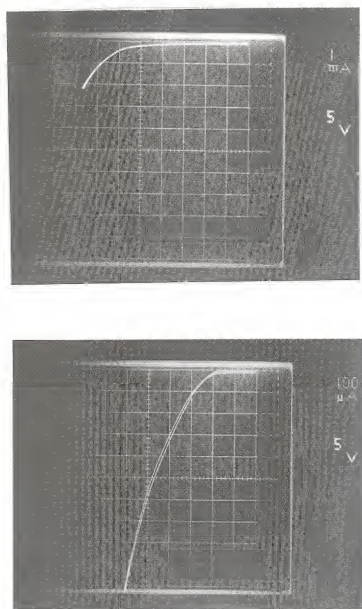


Figure 6.20 I-V characteristics of two Schottky barrier phase modulators on GaAs substrate with different lengths: 1.99 mm sample (top ) and 3.55 mm sample (bottom).

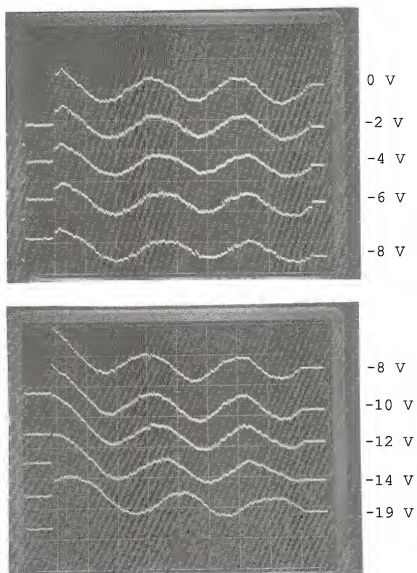


Figure 6.21 Lateral shifts of the fringe patterns under various applied reverse bias for 1.99 mm sample in a 2 V step.

change expected in the waveguide propagation constant  $\beta$  for a small perturbation of the refractive index  $n$  can be written by the first order perturbation theory as follows

$$\Delta\beta = \frac{k^2 \int_{-\infty}^{+\infty} n(x) \Delta n(x) |E_{OP}(x)|^2 dx}{\beta \int_{-\infty}^{+\infty} |E_{OP}(x)|^2 dx} \quad (6.3.1)$$

In our case,  $n(x)$  can be assumed to be constant and equals  $n_0$  in the guiding region so that  $kn_0 = \beta$ . Therefore, Eq. (6.3.1) can be rewritten by

$$\Delta N = \frac{\int_{-\infty}^{+\infty} \Delta n(x) |E_{OP}(x)|^2 dx}{\int_{-\infty}^{+\infty} |E_{OP}(x)|^2 dx} \quad (6.3.2)$$

, where  $\Delta N$  is the mode index change. Then phase shift is given by

$$\Delta\phi = \frac{2\pi L \Delta N}{\lambda} \quad (6.3.3)$$

For GaAs, when an applied electric field  $E(x)$  along the [001] direction, the refractive index change due to the linear electro-optic effect (or the Pockel's effect) is known to be

$$\Delta n_{LEO}(x) = \pm \frac{n_0^3}{2} r_{41} E(x) \quad (6.3.4)$$

where  $r_{41}$  is the LEO coefficient. The plus and minus signs corresponds to the  $[110]$  and  $[\bar{1}10]$  directions, respectively.

A propagating optical field experiences a different refractive index depending on its polarization and the propagation direction. For a TE mode propagating along the  $[\bar{1}10]$  direction, the refractive index increases since the electric component of the optical field is parallel to the  $[110]$  direction. For a TM mode polarized along the  $[001]$  direction, no refractive index change due to LEO effect occurs for an applied electric field along the  $[001]$  direction. From Eq.(6.3.3) and Eq.(6.3.4), the phase shift due to LEO effect can be written as

$$\Delta\phi_{LEO} = \pm \frac{\pi n^3}{\lambda} L r_{41} \{ \langle E(x) \rangle_{V_a} - \langle E(x) \rangle_0 \} \quad (6.3.5)$$

Here, the overlap integral  $\langle E(x) \rangle_{V_a}$  is defined by

$$\langle E(x) \rangle_{V_a} = \frac{\int_{-\infty}^{+\infty} [E(V_a, x)] |E_{op}(x)|^2 dx}{\int_{-\infty}^{+\infty} |E_{op}(x)|^2 dx} \quad (6.3.6)$$

, where  $E(V_a, x)$  is the electric field for the reverse bias voltage  $V_a$ ,  $L$  is the waveguide length and  $\lambda$  is the wavelength. A detailed derivation of the perturbation analysis is presented in Appendix B.

### 6.3.2 Analysis of phase shift for Schottky barrier phase modulator

Since the carrier concentration is very low in the guiding layer, one-sided abrupt  $p^+-n$  junction model is applicable to this Schottky barrier device. Then the depletion width  $W$  is given by [Sze81]

$$W = \sqrt{\frac{2\epsilon_s (V_i - V_a)}{qN_D}} \quad (6.3.7)$$

, where  $\epsilon_s$  : permittivity of GaAs

$q$  : electric charge of electron

$N_D$  : doping concentration

$V_i$  : built-in potential

$V_a$  : applied bias

Also the electric field distribution in the depletion region is given by [Sze81]

$$E(x) = \frac{qN_D(W-x)}{\epsilon_s} = E_m - \frac{qN_D x}{\epsilon_s} \quad (6.3.8)$$

, where  $x$  and  $E_m$  are the distance from the metal-contact and the maximum field strength is located at the metal-contact.

By use of Eq(6.3.5) and Eq(6.3.7), theoretical phase shifts at various applied reverse bias voltages were estimated. Theoretical overlap between the optical mode and the applied electric field at various reverse bias voltages is shown in Fig.6.22. Up to 8V reverse bias, the whole waveguide region is not fully depleted. In the theoretical calculation, a value of  $r_{41}=1.60 \times 10^{-10}$  cm/V was used. Detailed calculations for the phase shift are presented in appendix C. The theoretical results and experimental results are shown in Fig.6.23 and they are in excellent agreement. Theoretical results show that the slope (phase shift efficiency) is larger for the bias voltage less than 5V due to the rapid change of overlap between the optical mode and applied electric field. The phase shift at 4V reverse bias for the modulator on GaAs substrate is essentially the same for the modulator on Si substrate, considering the measurement error ( $\pm 2$  °/mm). By the comparison of the performance of both phase modulators on Si and GaAs substrate, it appears that the thermal stress effect on the LEO coefficient of GaAs-on-Si, which we inferred in the earlier reports [Kim89b, Kim90], does not seem to exist. In fact, the overlap between the modulating(bias) field and the optical field alone is able to explain the entire behavior of Schottky barrier phase modulator.



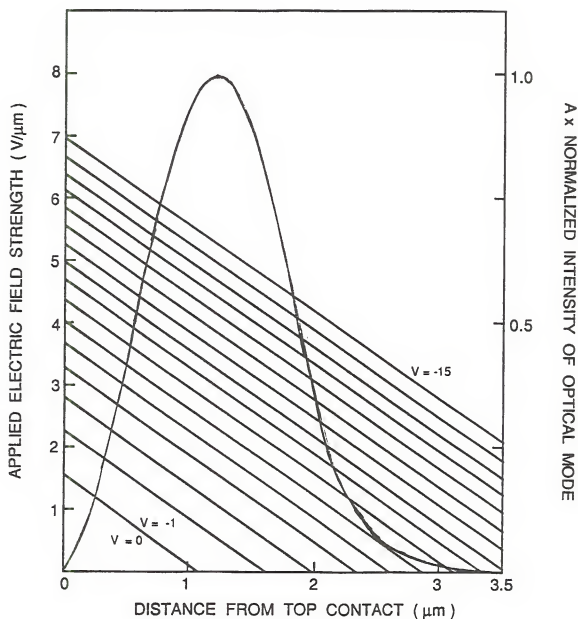


Figure 6.22 Theoretical overlap between optical mode and applied electric field distribution for Schottky barrier phase modulator. A is the normalized constant with a value of 1.3464. Straight lines are applied electric field distributions at different applied reverse bias.

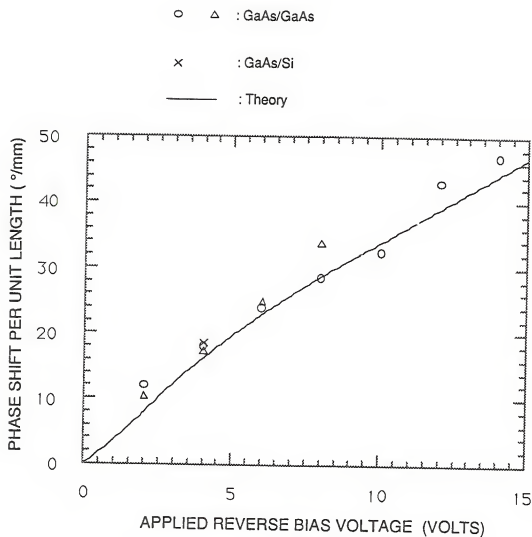


Figure 6.23 Comparison of theoretical results and experimental results for homoepitaxially and heteroepitaxially grown Schottky barrier phase modulator.

### 6.3.3 Analysis of p-N junction phase modulator grown by MBE

Although the structure itself is somewhat difficult to analyze due to the complexity of the Schottky contact and the p-N junction, to estimate the voltage drop across the damaged Schottky barrier, a similar theoretical analysis was carried out using the abrupt p-N junction. For the one-sided abrupt junction, the total depletion width is given by [Sze81]

$$W = \sqrt{\frac{2\epsilon_s(V_i - V_a)}{qN_A}} \quad (6.3.9)$$

,where  $N_A$  is the p-type carrier concentration. The calculated value of  $W$  is  $3.22 \times 10^{-4}$  cm for  $V_a = -6$  V. Also electric field distribution is given by

$$E(x) = E_m(1 - x/W) \quad (6.3.10)$$

,where  $x$  is the distance from the junction and  $E_m$  is the electric field strength at the junction for the applied bias. Considering the cross doping effect at the interface between GaAs and Si, actual p-N junction can be conveniently assumed to be located inside the  $\text{Al}_{0.05}\text{Ga}_{0.95}\text{As}$  layer. Therefore for the calculation purposes, two cases were considered. Junctions in these cases were assumed to be located as follows:

(A) junction at the GaAs-Si interface

(B) junction at  $0.3\text{ }\mu\text{m}$  away from the GaAs-Si interface

Here,  $0.3\text{ }\mu\text{m}$  as minimum cross doping depth was chosen based on the following reported results [Koha88, Hump88].

- (i) The reported cross doping depth of  $0.5\text{ }\mu\text{m}$  for GaP-on-Si measured by secondary ion mass spectroscopy (SIMS) depth profile.
- (ii) The interface defects of GaAs-on-Si are confined within  $0.3\text{ }\mu\text{m}$  from the interface.

For both cases of (A) and (B), the overlap between the optical mode and the applied electric field is shown in Fig6.24. Applied bias voltage was fixed at 6V for comparison with the experimental results. As before, a value of  $r_{41}=1.6\times 10^{-10}\text{cm/V}$  was used. Detailed calculations again are presented in Appendix C. The total phase shift of case (A) and case (B) were  $25.3^\circ$  and  $38.7^\circ$  for 1.65 mm length, respectively. Although it is very difficult analyze this complex modulator, the assumption of cross doping and the movement of junction inside the AlGaAs layer explain the experimental value of  $36^\circ$ , reasonably well.

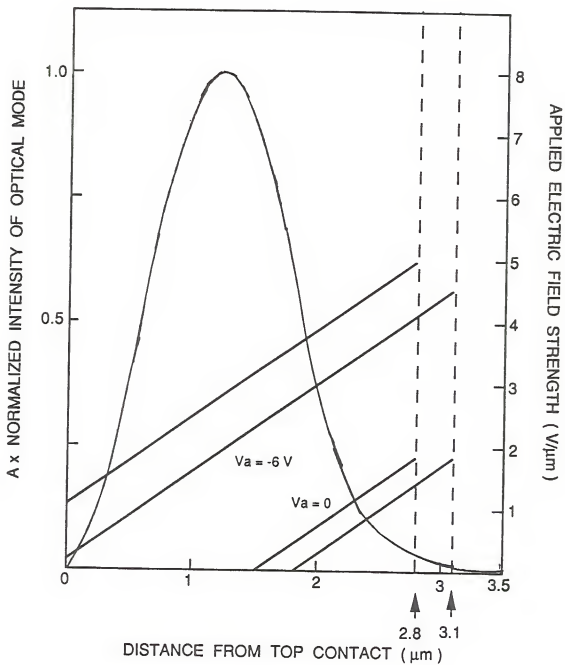


Figure 6.24 Theoretical overlap between optical mode and applied electrical field at 6V and zero reverse bias. Two junction locations at  $x = 2.8\ \mu\text{m}$  and  $x = 3.1\ \mu\text{m}$  are shown with dashed lines.

## CHAPTER SEVEN

### CONCLUSIONS

The growth of GaAs on Si substrate by metalorganic chemical vapor deposition and its applications to electrooptical devices such as waveguides and phase modulators have been studied. The results of this study are summarized in this chapter, followed by conclusions and recommendations for further study related to this subject are presented.

#### 7.1 Summary

GaAs-on-Si heterostructures have the potential to be one of the major material systems for future applications to OEIC's; It is especially useful in integrating both low and high speed electronic and electrooptical devices. The objective of the research project reported in this dissertation was to grow epitaxial GaAs layers on Si substrates applicable to electrooptical devices, and then fabricate, characterize, and analyze these devices.

A newly designed atmospheric pressure MOCVD system was constructed in order to get device-quality AlGaAs/GaAs

epitaxial layers. Several design considerations were investigated during the construction phase of the MOCVD system. Unique two-line configuration for the group III source delivery was adapted for the growth of various structures. In order to obtain abrupt interfaces, special features such as optimum locations of the massflow controllers, many-fold valve assembly and the differential pressure control in the vent-and-run mode were incorporated in the gas handling system. To obtain low doped materials, the following steps were taken: (i) use of fine electropolished tubings for reducing the memory effect, (ii) use of pure arsine, and (iii) adaptation of load-lock chamber.

For the optimization of growth parameters in the MOCVD system, various material characterizations such as measurements of Hall mobility, photoluminescence, carrier concentration, SEM, surface profile and surface morphology were carried out. The optimized main growth parameters were

total H<sub>2</sub> flow ; 10 slm

growth temperature ; 750 °C

V/III ratio ; 15 ~ 40

Optical device-quality GaAs on GaAs substrate with the background carrier concentration of  $n = 1.4 \times 10^{14} \text{ cm}^{-3}$  and an

electron mobility of  $\mu = 8100 \text{ cm}^2/\text{V}\cdot\text{sec}$  were obtained after the characterization of the MOCVD system.

For the growth of GaAs-on-Si by MOCVD, a two step growth technique was utilized. The thickness and growth temperature for GaAs buffer layer were critical factors in the two-step growth. The optimum temperature ranges for substrate annealing and growth of buffer layer were  $950 - 970^\circ\text{C}$  and  $400 - 450^\circ\text{C}$ , respectively. Among the various thicknesses of the GaAs buffer layers grown at low temperatures,  $200 \text{ \AA}$  buffer layer grown at  $425^\circ\text{C}$  showed the best quality with a mobility of  $\mu = 5700 \text{ cm}^2/\text{V}\cdot\text{sec}$ .

In order to characterize the thermal stress in GaAs-on-Si, thermally induced stress distribution were both measured and theoretically estimated using an appropriate analytical model. The measured stress of  $0.93 \times 10^9 \text{ dyne/cm}^2$  in the GaAs epitaxial layer alone grown on Si substrate was only half of the theoretical value at the growth temperature of  $320^\circ\text{C}$ . On the other hand, the measured stress distribution in Si substrate itself corresponds to the theoretical prediction. the conclusion is that the stress in the GaAs layer is linearly dependent on the growth temperature up to the threshold temperature of about  $320^\circ\text{C}$  and is independent of the growth temperature beyond its threshold temperature due to the stress release mechanism (propagation of dislocations) during the cooling process.



Towards achieving the objective of electrooptical device application of GaAs-on-Si, first optical waveguides followed by a p-N junction phase modulator grown by MBE were demonstrated. Moreover, a Schottky barrier phase modulator grown by our MOCVD system was characterized, and analyzed. For fabrication of these optical devices, the most critical and difficult step was the fabrication of mirror-like end facets for end-fire i.e., butt coupling of laser light. Cleaving after lapping the Si substrate down to about 30 - 40  $\mu\text{m}$  was proven to be suitable for this purpose.

With the heteroepitaxially grown GaAs ridge waveguides, propagation losses as low as 1.2 dB/cm were obtained for the fundamental TE mode. Further reductions of approximately 0.4 - 0.5 dB/cm in the propagation losses can be expected by increasing the cladding layer thickness. Additional loss, coming from scattering at ridge walls, could be improved by use of dry etching techniques. Our measurement and analysis of waveguides implies that the presence of a high density of dislocations ( about  $10^8 \text{ cm}^{-2}$  ) in the GaAs layer on Si does not significantly affect the loss of the waveguide.

Schottky and p-N junction phase modulators were also fabricated and phase efficiencies of 4.7  $^\circ/\text{V}\cdot\text{mm}$ , and 3.5  $^\circ/\text{V}\cdot\text{mm}$ , respectively, were demonstrated. For the purpose of comparison, a Schottky type modulator on GaAs substrate was also fabricated and characterized. In addition theoretical modeling of Schottky type modulator was performed. Experimental results for both the modulators on GaAs as well

as Si substrates were shown to be in excellent agreement with the theoretical results. This indicates that the suspected thermal stress effect on the LEO coefficient of GaAs-on-Si seems to be negligible. Although the obtained phase shift efficiency for the GaAs/Si was comparable to that of GaAs/GaAs, the achievable maximum total phase shift on Si was far less than that on GaAs because of the lower reverse break-down voltage of the Schottky barrier. This low break-down voltage is mainly due to the high density of dislocations, which is one of current problems that needs to be overcome in GaAs-on-Si research area.

For the p-N junction modulator on Si, our analysis indicates that the cross doping effect at GaAs/Si interface ( diffusion of Si atoms into the epitaxial layer ) is probably responsible for the rather high value of phase shift efficiency as compared to the theoretical value.

## 7.2 Recommendations for Further Study

### Growth

According to the experience, the cleaning procedure and isolation of the cleaned substrate from the air were critical factors for the growth of GaAs-on-Si. Especially the transferring mechanism for the cleaned Si substrate in the non-reactive gas (  $H_2$ ,  $N_2$ , or Ar ) to the load-lock chamber would improve the quality of the grown film. Other buffer layers with proper thermal expansion coefficient can be used

in order to reduce the wafer bending. As an example, the use of SOI( such as silicon on Sapphire) has already been proposed. For this purpose, search for the proper materials as buffer layers is necessary to advance the GaAs/Si technology..

#### Fabrication process

For electrooptical devices, a refined etching technique to define the ridge structure and a fast and convenient technique for facet preparation are necessary. Some advanced techniques such as RIE(reactive ion etching) and plasma etching must be utilized to obtain smooth ridge walls. For integration of several devices using GaAs-on-Si system, new facet preparation techniques should be developed. Some special etching technique capable producing mirror-like facets, rather than current cleaving method is desirable.

#### Electrooptical devices

Our study indicates that low loss waveguides for passive device applications of GaAs/Si can be grown with performance comparable to that on GaAs substrates. Furthermore, we have demonstrated that GaAs/Si modulators, in particular, Schottky barrier modulators, perform as well as identical GaAs heterostructure devices grown on GaAs substrates. The thermally induced stress does not seem to affect the electrooptic effect. The limitation, however, seems to be the lower reverse breakdown voltage which is inherently limited by the high density of dislocations. Incorporation of

strained layer superlattices as buffers will help releasing the stress so that dislocations do not travel vertically, rather are propagated horizontally. This should avoid the problem of low reverse break-down voltage due to the high dislocation density. Particularly for the phase modulator, highly efficient structures such as p-n junction, p-i-n, and PpinN structure rather than Schottky barrier are better choices for the application of GaAs-on-Si material system.

## APPENDIX A

### THEORETICAL CALCULATION OF THERMAL RESIDUAL STRESS

The model of stress distribution is based on the following assumptions for the schematic deformation given in Fig.A.1;

- i) GaAs and Si are isotropic.
- ii) The bond between Si and GaAs are perfect.
- iii) Shear deformation (ABCD line in Fig.A.1 is straight and perpendicular to midplane of the wafer, and remains same in the deformed state)
- iv) One-dimensional stress distribution is considered.
- v) Change in the normal direction is insignificant comparing to displacement  $w_0$ .
- vi) The point B at the geometric midplane undergoes displacements  $u_0$ ,  $v_0$ , and  $w_0$  along x, y, and z directions, respectively.

The displacement  $u$  in the x direction of a point C that is located on the normal ABCD at a distance  $z$  from the midplane is given by

$$u = u_0 - z\alpha \quad (\text{A.1})$$

, where  $\alpha$  is the slope of the midplane in the x direction, that is,

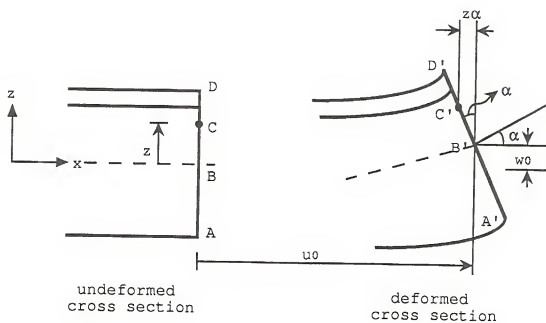


Figure A.1 Model for the analysis of thermal stress in GaAs-on-Si: thin top layer is GaAs.

$$\alpha = \frac{\delta w_0}{\delta x} \quad (\text{A.2})$$

Therefore

$$u = u_0 - z \frac{\delta w_0}{\delta x} \quad (\text{A.3})$$

By similar reasoning, the displacement  $v$  in the  $y$  direction of an arbitrary point at a distance  $z$  from the midplane is

$$v = v_0 - z \frac{\delta w_0}{\delta x} \quad (\text{A.4})$$

By the assumption (v),

$$w = w_0 \quad (\text{A.5})$$

Considering  $x$ ,  $z$  directions only, by assumptions (iv) and (v),

$$\begin{aligned} \epsilon_x &= \frac{\delta u}{\delta x} = \frac{\delta u_0}{\delta x} - z \frac{\delta^2 w_0}{\delta x^2} \\ \epsilon_z &= \frac{\delta w_0}{\delta z} = 0 \end{aligned} \quad (\text{A.6})$$

Defining  $\epsilon_0$  and  $k_0$  as midplane strain and midplane curvature, respectively, we can write above relations in a simple form

$$\epsilon_x = \epsilon_0 + k_0 z \quad (\text{A.7})$$

Thus, the stress-strain relation for deformed geometry is given by

$$\sigma = \frac{E}{1 - \nu^2} (\epsilon_0 + k_0 z) \quad (\text{A.8})$$

, where E: Young's modulus

$\nu$ : Poisson's ratio

And thermal strain is given by

$$\epsilon^T = \alpha \Delta T \quad (\text{A.9})$$

, where  $\alpha$ : thermal expansion coefficient difference

$\Delta T$ : temperature change

Here, thermal strains do not produce a resultant force or moment when the body (GaAs + Si) is completely free to expand, bend, and twist. When a GaAs-on-Si as a whole is considered, a temperature change does not affect the resultant force or moment. However, an individual layer is not completely free to deform due to the difference of thermal expansion coefficients of GaAs and Si. Its deformation is influenced by other layer. Therefore the stresses in a GaAs-Si are produced only by the strains that are in excess of the thermal strains for its free expansion



given by Eq.(A.9). Hence, from Eq.(A.7) and Eq.(A.9), the strain that causes stress is given by

$$\begin{aligned}\epsilon^M &= \epsilon_x - \epsilon^T \\ &= \epsilon_0 + z k_0 - \alpha \Delta T\end{aligned}\tag{A.10}$$

Then the induced thermal stress in the layer is

$$\sigma^T = \frac{E}{1 - \nu^2} (\epsilon_0 + z k_0 - \alpha \Delta T)\tag{A.11}$$

Generally, considering n-layer case as shown in Fig.A.2, the resultant force and moment acting on the cross section are expressed as

$$N = \sum_{k=1}^n \int_{h_{k-1}}^{h_k} \sigma \, dz\tag{A.12}$$

$$M = \sum_{k=1}^n \int_{h_{k-1}}^{h_k} \sigma z \, dz\tag{A.13}$$

, where N and M are resultant force and moment, respectively. In our case,  $N = 0$  and  $M = 0$  for  $s = s^T$ . Therefore, we have

$$\begin{aligned}\sum_{k=1}^n [E_k \epsilon_0 (h_k - h_{k-1}) + \frac{E_k k_0}{2} (h_k^2 - h_{k-1}^2)] \\ = \Delta T \sum_{k=1}^n E_k \alpha_k (h_k - h_{k-1})\end{aligned}\tag{A.14}$$

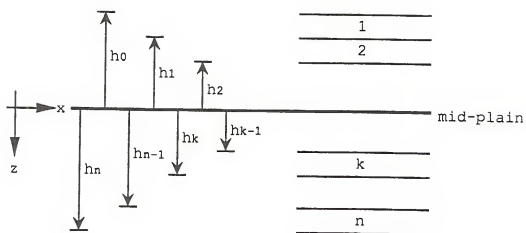


Figure A.2 Multilayered structure.

$$\begin{aligned}
 \sum_{k=1}^n \left[ \frac{E_k \epsilon_0}{2} (h_k^2 - h_{k-1}^2) + \frac{E_k k_0}{3} (h_k^3 - h_{k-1}^3) \right] \\
 = \frac{\Delta T}{2} \sum_{k=1}^n E_k \alpha_k (h_k^2 - h_{k-1}^2)
 \end{aligned}
 \quad (A.15)$$

From Eq. (A.14) and (A.15),  $\epsilon_0$  and  $k_0$  are determined and thermal stress distribution in  $i$ -th layer along  $z$  becomes

$$\sigma_i^T = E_i (\epsilon_0 + z k_0 - \alpha_i \Delta T) \quad (A.16)$$

For the calculation of  $\sigma_i^T$  in our case, the following numerical values were used.

$$E_{\text{GaAs}} = 0.855 \times 10^{12} \text{ dynes/cm}^2$$

$$E_{\text{Si}} = 1.310 \times 10^{12} \text{ dynes/cm}^2$$

$$\nu_{\text{GaAs}} = 0.55$$

$$\nu_{\text{Si}} = 0.2786$$

$$\alpha_{\text{GaAs}} = 6.0 \times 10^{-6} / ^\circ\text{C}$$

$$\alpha_{\text{Si}} = 2.5 \times 10^{-6} / ^\circ\text{C}$$

$$d_{\text{GaAs}} = 2 \text{ } \mu\text{m}$$

$$d_{\text{Si}} = 150 \text{ } \mu\text{m}$$

$$\Delta T = 650 \text{ } ^\circ\text{C}$$

# APPENDIX B DERIVATION OF $\Delta\beta$

For asymmetrical slab waveguide, (6.3.1) is derived from the Helmholtz wave equation by the first order perturbation theory. Let's assume the one dimensional unperturbed Helmholtz equation written in the form of

$$\frac{\partial^2 \psi(x)}{\partial x^2} + \{n(x)^2 k^2 - \beta^2\} \psi(x) = 0 \quad (B.1)$$

where  $\psi(x)$  : optical field profile

$n(x)$  : refractive index of grinding region

$k$  : propagation constant in free space

$\beta$  : effective propagation constant.

Suppose that this equation has been solved, the field profile  $\psi(x)$  has been found and  $\beta$  has been determined. Suppose next that  $n(x)$  is now changed from  $n(x)$  to  $n(x) + \Delta n(x)$ . Then the new effective propagation constant and the new field profile are  $\beta + \Delta\beta$  and  $\psi(x) + \Delta\psi(x)$ , respectively. An perturbed wave equation for the perturbation  $\Delta n(x)$  can be written in

$$\frac{d^2}{dx^2} (\psi + \Delta\psi) + [(n + \Delta n)^2 k^2 - (\beta + \Delta\beta)^2] (\psi + \Delta\psi) = 0 \quad (B.2)$$

Using the first order approximation  $(\Delta n)^2 \cong 0$ ,  $(\Delta\beta)^2 \cong 0$ , and  $(\Delta\beta)(\Delta\psi) \cong 0$  and (B.1),

$$\frac{d^2}{dx^2} (\Delta\psi) + (2nk^2\Delta n\psi + n^2k^2\Delta\psi) - (2\beta\Delta\beta\psi + \beta^2\Delta\psi) = 0 \quad (B.3)$$

Multiplying (B.3) by  $\psi^*$  and integrating over  $-\infty < x < \infty$ ,

$$\begin{aligned} 2\beta\Delta\beta \int_{-\infty}^{\infty} dx |\psi|^2 &= 2k^2 \int_{-\infty}^{\infty} dx n \Delta n |\psi|^2 \\ + \int_{-\infty}^{\infty} dx \left[ \psi^*(x) \frac{d^2(\Delta\psi)}{dx^2} + n^2 k^2 \psi^* \Delta\psi - \beta^2 \psi^* \Delta\psi \right] \end{aligned} \quad (B.4)$$

For the second integral on the right hand side, using the following relation:

$$\frac{d}{dx} \left[ \psi^* \frac{d}{dx} (\Delta\psi) - \Delta\psi \frac{d}{dx} \psi^* \right] = \psi^* \frac{d^2(\Delta\psi)}{dx^2} - \Delta\psi(x) \frac{d^2\psi^*}{dx^2} \quad (B.5)$$

then,

$$\begin{aligned} \int_{-\infty}^{\infty} dx \psi^* \frac{d^2(\Delta\psi)}{dx^2} &= \int_{-\infty}^{\infty} \frac{d}{dx} \left[ \psi^* \frac{d}{dx} (\Delta\psi) - \Delta\psi \frac{d}{dx} \psi^* \right] dx \\ &+ \int_{-\infty}^{\infty} dx \Delta\psi(x) \frac{d^2\psi^*}{dx^2} \end{aligned} \quad (B.6)$$

At  $x = \pm\infty$ ,  $\psi^*(x)$  and  $\Delta\psi(x)$  vanishes. Therefore, (B.6) can be written by

$$\int_{-\infty}^{\infty} dx \psi^* \frac{d^2(\Delta\psi)}{dx^2} = \int_{-\infty}^{\infty} dx \Delta\psi(x) \frac{d^2\psi^*}{dx^2} \quad (B.7)$$

By use of (B.7), (B.4) becomes

$$2\beta\Delta\beta\int_{-\infty}^{\infty}dx|\psi|^2 = 2k^2\int_{-\infty}^{\infty}dxn\Delta n|\psi|^2 + \int_{-\infty}^{\infty}dx\left[\left(\frac{d^2\psi^*}{dx^2} + (n^2k^2 - \beta^2)\psi^*\right)\Delta\psi\right] \quad (\text{B.8})$$

From (B.1), assuming that  $\beta$  is real,

$$\frac{d^2\psi^*}{dx^2} + (n^2k^2 - \beta^2)\psi^* = 0$$

Therefore, from (B.8), we obtain the perturbation formula for  $\Delta\beta$ , which is (6.3.1),

$$\Delta\beta = \frac{k^2\int_{-\infty}^{\infty}dxn\Delta n|\psi|^2}{\beta\int_{-\infty}^{\infty}dx|\psi|^2} \quad (\text{B.9})$$

# APPENDIX C

## THEORETICAL CALCULATION OF PHASE SHIFT

For the calculation of phase shift, it is obvious to do the overlap integral defined by Eq.(6.3.5). For the overlap integral, the intensity profile of the optical mode and the applied electric field distribution should be known for the particular device structure.

### Intensity profile for the fundamental mode( $TE_0$ )

As seen in Fig.6.2.(a), the mode is well guided single mode(  $TE_0$  ) in our phase modulator structure. Therefore, three layer asymmetric slab waveguide model is sufficient to get the intensity distribution. In the asymmetric waveguide shown in Fig.C.1, let  $p$  be the distance from the air-GaAs interface to the location of the field maximum. Then,  $2-p$  is the distance from the GaAs-AlGaAs interface to the location of the field maximum. If the location of the air-GaAs interface is  $x = 0$ , the field distribution of the mode is given by[Case78]

$$\begin{aligned} E_y(x) &= A_e \cos(k_f p) \exp\{\gamma_a x\} & \text{for } x < 0 \\ E_y(x) &= A_e \cos\{k_f(x-p)\} & \text{for } 0 < x < 2 \\ E_y(x) &= A_e \cos\{k_f(2-p)\} \exp\{-\gamma_b(x-2)\} & \text{for } x > 2 \end{aligned} \quad (C.1)$$

, where

$$k_f^2 = k^2(n_f^2 - N^2)$$

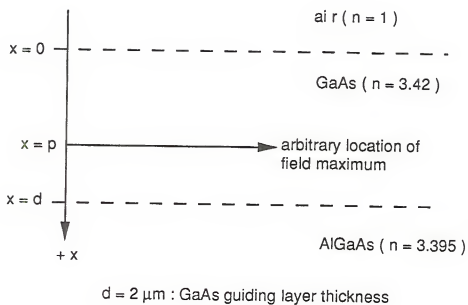


Figure C.1 Slab waveguide model



$$\gamma_b^2 = k^2(N^2 - n_b^2)$$

$$\gamma_a^2 = k^2(N^2 - n_a^2)$$

$$k = 2\pi/\lambda$$

Here  $N$  is the effective mode index and  $n_f$ ,  $n_b$ , and  $n_a$  are the refractive indices of GaAs,  $\text{Al}_{0.05}\text{Ga}_{0.95}$ , and air, respectively. By using Eq.(6.1.1) through Eq.(6.1.4),  $k_f$ ,  $\gamma_b$ , and  $\gamma_a$  at  $\lambda = 1.3 \mu\text{m}$  can be determined and have the numerical values as follows

$$k_f = 1.20750 \mu\text{m}^{-1}$$

$$\gamma_b = 1.58805 \mu\text{m}^{-1}$$

$$\gamma_a = 15.7610 \mu\text{m}^{-1}$$

From the zigzag-ray model for the asymmetric three layer slab waveguide,  $p$  can be expressed by [Case78]

$$p = 2 - \{\tan^{-1}(\gamma_b/k_f)\}/k_f \quad (\text{C.2})$$

Therefore, the numerical value is  $p = 1.23752$ . Thus all the informations about the optical mode are known.

### Applied electric field distribution

#### (i) Schottky barrier phase modulator

From Eq.(6.3.7), for doping concentration of  $10^{15} \text{ cm}^{-3}$ , the GaAs and AlGaAs layer is fully depleted at  $V_a = -7.8 \text{ V}$ . For the calculations, dielectric constant 12.85 for GaAs [Will84] and  $V_i = 0.86$  [Sze81] were used. Therefore, as

shown in Fig.C.2, two different kinds of applied field distribution should be considered.

For  $V_a > -7.8$  V ( $W < 3.5$   $\mu\text{m}$ ), since shaded area is equal to  $V_i + V_a$ ,  $E_m$ (maximum applied electric field strength) is given by

$$E_m = 2 (V_i + V_a) / W \quad (\text{C.3})$$

Defining the applied electric field distribution in the coordinate system given in Fig.C.2 as

$$E(x) = Ax + B \quad (\text{C.4})$$

then, by Eq.(6.3.7) and Eq. (C.5),

$$A = - \frac{E_m}{W} = - \frac{qNd}{\epsilon_s} \quad (\text{C.5})$$

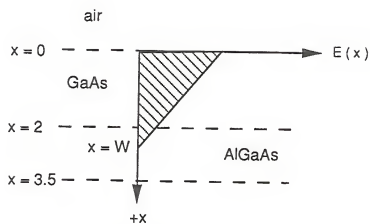
$$B = E_m \quad (\text{C.6})$$

The calculated value of A is -1.41 .

For  $V_a < -7.8$  V ( $W = 3.5$   $\mu\text{m}$ ), from Fig.C.2.(b),

$$B = (V_a + V_i) / 3.5 + 2.4675 \quad (\text{C.7})$$

(a)



(b)

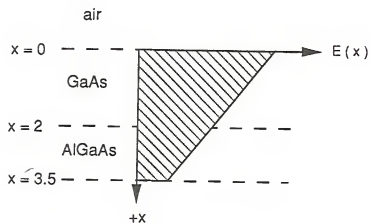


Figure C.2 Applied electric field distributions in each cases: (a) for  $W < 3.5 \mu\text{m}$  (b) for  $W = 3.5 \mu\text{m}$ .

(ii) Abrupt p-N junction phase modulator

From Eq.(6.3.8), for  $N_A \sim 10^{15} \text{cm}^{-3}$  and  $V_i = 1,2 \text{V}$  [Sze81], depletion widths at  $V_a = 0$  and  $V_a = -6 \text{ V}$  are  $1.30 \mu\text{m}$  and  $3.22 \mu\text{m}$ , respectively. In the coordinate used in Fig.6.24, by the same method used for Schottky barrier phase modulator, the applied field distribution can be obtained for each junction location at  $V_a = 0 \text{ V}$  and  $V_a = -6 \text{ V}$ .

For junction location at  $x = 3.1$ ,

$$\begin{aligned} E(x) &= 1.412x - 2.537 & \text{for } V_a = 0 \\ E(x) &= 1.412x + 0.135 & \text{for } V_a = -6 \text{ V} \end{aligned} \quad (\text{C.8})$$

For junction location at  $x = 2.8$ ,

$$\begin{aligned} E(x) &= 1.412x - 2.113 & \text{for } V_a = 0 \\ E(x) &= 1.412x - 0.924 & \text{for } V_a = -6 \text{ V} \end{aligned} \quad (\text{C.9})$$

#### Overlap integral $\langle E \rangle_{V_a}$

Denominator of  $\langle E \rangle_{V_a}$  defined in Eq.(6.3.6) can be calculated by using Eq.(C.1) as follows;

$$\begin{aligned} \int_{-\infty}^{+\infty} |E_{op}(x)|^2 dx &= \int_{-\infty}^0 |E_y(x)|^2 dx + \int_0^2 |E_y(x)|^2 dx + \int_2^{+\infty} |E_y(x)|^2 dx \\ &= 1.3464 A_e^2 \end{aligned} \quad (\text{C.10})$$

(i) Schottky barrier phase modulator

For the calculation of numerator of  $\langle E \rangle_{V_a}$ , three different cases of the applied reverse bias voltage should be considered as follows:

(a)  $V_a > -1.97 \text{ V}$  ( $W < 2 \mu\text{m}$ )

$$(b) -7.80 \text{ V} < V_a < -1.97 \text{ V} \quad (2 \text{ } \mu\text{m} < W < 3.5 \text{ } \mu\text{m})$$

$$(c) V_a < -7.80 \text{ V} \quad (W = 3.5 \text{ } \mu\text{m})$$

$$(a) \text{ For } V_a > -1.97 \text{ V} \quad (W < 2 \text{ } \mu\text{m}),$$

$$\begin{aligned} & \int_{-\infty}^{\infty} E(x) |E_{op}(x)|^2 dx \\ &= \int_0^W E(x) |E_y(x)|^2 dx \\ &= \int_0^W dx [Ax + B] [Ae^2 \cos^2(k_f(x-p))] \\ &= Ae^2 \left[ A \left[ \frac{W^2}{4} + \frac{W}{4k_f^2} \sin(2k_f(W-p)) + \frac{1}{8k_f^2} (\cos(2k_f(W-p)) - \cos(2k_f p)) \right] \right. \\ & \quad \left. + B \left[ \frac{W}{2} + \frac{1}{4k_f} (\sin(2k_f(W-p)) + \sin(2k_f p)) \right] \right] \end{aligned} \quad (C.11)$$

$$(b) \text{ For } -7.80 \text{ V} < V_a < -1.97 \text{ V} \quad (2 \text{ } \mu\text{m} < W < 3.5 \text{ } \mu\text{m})$$

$$\begin{aligned} & \int_{-\infty}^{\infty} E(x) |E_{op}(x)|^2 dx \\ &= \int_0^2 E(x) |E_y(x)|^2 dx + \int_2^W E(x) |E_y(x)|^2 dx \end{aligned}$$

$$\begin{aligned}
&= A_0^2 \left[ A \left\{ 0.0994 + \frac{\cos^2(k_d(2-p))}{2\gamma_s} \left( \left( 1 + \frac{1}{2\gamma_s} \right) e^{2\gamma_s(2-w)} \left( w + \frac{1}{2\gamma_s} - 1 \right) \right) \right\} \right. \\
&\quad \left. + B \left[ 1.2311 + \frac{\cos^2(k_d(2-p))}{2\gamma_s} (1 - e^{2\gamma_s(2-w)}) \right] \right]
\end{aligned}
\tag{C.12}$$

(c)  $V_a < -7.80 \text{ V}$  ( $W = 3.5 \text{ } \mu\text{m}$ ),

$$\begin{aligned}
&\int_{-\infty}^{\infty} E(x) |E_{op}(x)|^2 dx \\
&= \int_0^2 E(x) |E_y(x)|^2 dx + \int_2^{3.5} E(x) |E_y(x)|^2 dx
\end{aligned}$$

$$= A_0^2 (0.2483 A + 1.380 B) \tag{C.13}$$

Therefore  $\langle E \rangle_{V_a}$  can be obtained by use of (C.10), (C.11), (C.12), (C.13) and values of A and B in (C.5), (C.7) and (C.9). For example,

$$\langle E \rangle_{V_a=0} = 0.1842 \text{ (V/}\mu\text{m)}$$

$$\langle E \rangle_{V_a \geq 8} = 0.293 V_a + 1.076 \text{ (V/}\mu\text{m)}$$

Thus from Eq.(6.3.5), the phase shift  $\Delta\phi$  can be calculated for applied reverse bias  $V_a$ .

(ii) Abrupt p-N junction phase modulator

Denominator of  $\langle E \rangle_{V_a}$  has the same value of  $1.3464 A_0^2$ .

For junction at  $x = 3.2$ ,

$$\int_{-\infty}^{+\infty} E(x) |E_{0H}|^2 dx = \int_0^2 E(x) |E_{0H}|^2 dx + \int_2^{3.2} E(x) |E_{0H}|^2 dx$$

Therefore, using Eq. (C.8) and Eq. (C.1),

$$\langle E \rangle_{V_a=6} = 1.7966 \text{ V}/\mu\text{m}$$

$$\langle E \rangle_{V_a=0} = 0.0677 \text{ V}/\mu\text{m}$$

For junction at  $x = 2.8$ ,

$$\int_{-\infty}^{+\infty} E(x) |E_{0H}|^2 dx = \int_0^2 E(x) |E_{0H}|^2 dx + \int_2^{2.8} E(x) |E_{0H}|^2 dx$$

Thus, by Eq. (C.9) and (C.1),

$$\langle E \rangle_{V_a=6} = 2.7820 \text{ (V}/\mu\text{m)}$$

$$\langle E \rangle_{V_a=0} = 0.1334 \text{ (V}/\mu\text{m)}$$

Therefore, the values  $\Delta\phi$  given in subsection 6.3.3 are obtained.

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